KU LEUVEN

ARENBERG DOCTORAL SCHOOL
Faculty of Science

Defect generation at interfaces of Ge-based high mobility semiconductors with oxide insulators

Oreste Madia

Promoter:
Prof. Dr. V.V. Afanas'ev

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor in Science: Physics

September 2016

Defect generation at interfaces of Ge-based high mobility semiconductors with oxide insulators

Oreste MADIA

Examination committee:
Prof. Dr. M. Wübbenhorst, Chairman
Prof. Dr. V.V. Afanas'ev, Promoter
Prof. Dr. A. Stesmans, Co-supervisor
Prof. Dr. M. Houssa
Prof. Dr. G. Adriaenssens
Dr. D. Buca (Fz-Juelich)
Dr. B. Kaczer (Imec)

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor in Science: Physics

September 2016

Uitgegeven in eigen beheer, Oreste Madia, Celestijnenlaan 200D, B-3001 Leuven (Belgium)

A mamma, papà e Maty

Abstract

Further advance of the microelectronic devices performance will soon require the use of a semiconducting materials with charge carrier mobilities significantly higher than those of silicon. Among the feasible conditions, Ge has repeatedly been indicated as one of the most promising options because both electron and hole mobilities in bulk Ge are larger than in silicon, while SiGe alloys have already been implemented in the CMOS process since 2003. The latter implies that the future use of Ge will encounter reduced process adaptation costs as compared to other semiconducting materials, such as $A_{III}B_{V}$ group materials. Unfortunately, high densities of electrically active defects found at interfaces of Ge-based semiconductors with oxide insulators causing degraded device performance and reliability remain an unsolved issue. Therefore, understanding the origin of these charge traps is critical to enable the successful implementation of Ge in MOSFET technology.

In this thesis work we combine several experimental characterization techniques to obtain information concerning the atomic origin and electrical behavior of relevant defects in several (Si)Ge-based technologies.

We have found that, depending on the Ge concentration and strain configuration, interfaces between SiGe layers and oxide insulators can contain defects exclusively associated with dangling bonds of Si or Ge atoms. It also appears possible that, by appropriately tailoring the Ge concentration and residual strain in SiGe layers, one can obtain defect-free interfaces with SiO_2.

Further, we confirm that the major source of electrically active defects in Ge / high-k stacks stems from defects inside the oxide insulator. The time response of these defects is much larger than the one from interface states and, as a result, the conventional room-temperature capacitance and conductance methods are largely unable to probe them. By contrast, the advanced Saturation surface PhotoVoltage technique allows for more reliable estimations of the interface trap density (D_{IT}). Finally, we have found that a significant additional contribution

to the D_{IT} encountered at interfaces of Ge with high-k oxide insulators correlates with the presence of Ge contaminants in the oxide. The latter suggests the need of introducing an additional barrier layer to prevent out-diffusion of Ge from the channel region.

Globally seen, the dominance of the oxide traps and low density of Ge dangling bond defects represent the major difference between the Ge / oxide interfaces and the Si / oxide entities.

Beknopte samenvatting

De verdere vooruitgang van de microelektronische systemen zal snel afhangen van het gebruik van halfgeleider materialen met een significant hogere ladingsdrager mobiliteit dan deze van silicon.

Vantussen de uitvoerbare opties is Ge herhaaldelijk aangewezen als één van de meest veelbelovende opties want zowel de elektronen- als de gatenmobiliteit in bulk Ge zijn groter dan in silicon, onderwijl zijn SiGe legeringen reeds in CMOS processen geïmplementeerd sinds 2003. Het laatstgenoemde impliceert dat in de toekomst Ge zal genieten van verminderde proces aanpassingskosten vergeleken met andere halfgeleider materialen, zoals bijvoorbeeld de groep III-V materialen.

Helaas, de hoge dichtheid van elektrisch actieve defecten, gevonden aan de grensvlakken tussen Ge-gebaseerde halfgeleiders en oxide insulatoren, welke de prestatie en de betrouwbaarheid verminderen, blijven een onopgelost probleem. Daarom is het bevatten van de oorsprong van deze ladings vallen cruciaal voor de implementatie van Ge in MOSFET transistor technologie.

In deze thesis combineren we verschillende experimentele karakterisatie technieken om informatie te vergaren over de atomische oorsprong and het elecktrische gedrag van de relevante defecten in meerdere (Si)Ge-gebaseerde technologiën. We hebben gevonden dat, afhankelijk van de Ge-concentratie and de spanningsconfiguratie, de grensvlakken tussen de SiGe lagen en de oxide insulatoren enkel defecten bevatten geassociëerd met ongepaarde bindingen van de Si of Ge atomen. Het lijkt eveneens mogelijk dat, door de Ge-concentratie en

de overgebleven spanning in de SiGe lagen op scherp te stellen, men defect-vrije grenslagen met SiO_2 kan verkrijgen.

Verder hebben we bevestigd dat de grootste bron van elektrisch actieve defecten in Ge / hoge-k stapels afstamt van defecten vanbinnen de oxide insulator. De tijdsresponse van deze defecten is veel groter dan van grensvlak staten, en als resultaat zijn conventionele kamertemperatuur capaciteits- en geleidingsmethoden grotendeels niet in staat deze te meten. In contrast, verschaft de geavanceerde Verzadigings oppervlakte FotoVoltage techniek meer betrouwbare D_{IT} schattingen.

Als laatste hebben we gevonden dat er een significante bijkomende bijdrage aan de D_{IT}, gelegen aan grensvlakken tussen Ge en de hoge-k oxide insulatoren, correleert met de aanwezigheid van Ge vervuilers in de oxide. Het laatstgenoemde suggereert een nood aan introductie van een aanvullende barriérelaag om Ge diffusie vanuit het kanaalgebied te voorkomen. Globaal gezien, presenteert de dominantie van de oxide vallen en de lage dichtheid van Ge ongepaarde bindingsdefecten het grootste verschil tussen de Ge / oxide grensvlakken en de Si / oxide instanties.

Contents

Abstract g

Contents k

List of abbreviations n

List of symbols q

1 The evolution of semiconductor devices and the role of defects 1

1.1 CMOS technology - Device scaling and the era of disruptive innovations 2

1.2 Alternative channel materials - Ge and Ge-based alloys as a replacement for Si 6

1.3 Challenges for the use of Ge-based channel materials 7

1.4 Reliability issues in MOS devices - Bias Temperature Instability 10

1.5 Rationale of this work 14

2 Experimental techniques 21

2.1 Admittance response of MOS capacitors 22

2.1.1 CV and GV characterization 25

2.1.2 AC conductance method and solution of the Berglund integral 27

2.1.3 Gray-Brown method 30
2.2 Saturation surface PhotoVoltage 31
2.3 Exhaustive PhotoDepopulation Spectroscopy 35
2.4 Electron Spin Resonance 38
2.5 Positron Annihilation Spectroscopy 40

3 Ge P_{b1} centers at interfaces of condensation-grown SiGe layers with SiO_2 47

3.1 The Si dangling bond defect 48
3.2 The Ge dangling bond defect 50
3.3 The Ge-condensation growth method 52
3.4 Impact of strain on generation and passivation of Ge P_{b1} centers 53
3.5 Charge transition level of Ge P_{b1} centers 58

4 Defect density reduction in Si-passivated epi-SiGe channel devices with HfO_2 insulator 73

4.1 Samples description, preparation, and characterization details . 74
4.2 Reduction of Si P_{b0} centers in Si-passivated SiGe MOS devices caused by Ge out-diffusion 78

5 Ge / oxide interface traps: Fast versus slow states 87

5.1 Limitations of conventional trap characterization techniques for high-mobility semiconductor / high-k insulator stacks 88
5.2 Interface trap characterization in Ge/Sc-doped GeO_2/HfO_2 structures by SPV and AC conductance measurements 89
5.3 Defect densities at Ge/high-k interfaces studied by the SPV method 93

6 Intrinsic and Ge-related deep electron traps in ALD-grown HfO_2 99

7 Conclusions and Outlook 113

A Validation and control measurements on the SPV set up **119**

A.1 Si/SiO_2 D_{IT} determination 120

A.2 Impact of buried interfaces on the SPV measurements 122

A.3 Impact of Dember potential studied on $InP/In_{0.53}Ga_{0.47}As/GdAlO_3/HfO_2$ capacitors 126

A.4 Impact of strong Fermi level pinning 128

List of publications **133**

n

List of abbreviations

AC	Alternating Current
ALD	Atomic Layer Deposition
BOX	Buried OXide
BTI	Bias Temperature Instability
CB	Conduction Band
CBB	Conduction Band Bottom
CMOS	Complementary-MOS
CV	Capacitance - Voltage
Db	Doppler broadening
DB	Dangling Bond
DC	Direct Current
EOT	Equivalent Oxide Thickness
EPDS	Exhaustive Photo Depopulation Spectroscopy
ESR	Electron Spin Resonance
FET	Field-Effect Transistor
FINFET	Fin-shaped FET
GOI	Germanium-On-Insulator
GST	Generalized Simple Thermal
GV	Conductance - Voltage
HF	High Frequency
IL	Inter-Layer
IPE	Internal Photo Emission
IT	Information Technology
HF	HydroFluoric acid
HK	High-k
HKMG	High-k Metal Gate
HR-XRD	High-Resolution X-Ray Diffraction
LCR	Inductance, Capacitance, and Resistance
LF	Low Frequency
ML	Mono-Layer
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NBTI	Negative BTI

PA	Positron Annihilation
PAS	Positron Annihilation Spectroscopy
PBTI	Positive BTI
PC	PhotoConductivity
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PV	PhotoVoltage
QW	Quantum well
RBS	Rutherford Back Scattering
RPCVD	Reduced Pressure Chemical Vapor Deposition
SCD	Spectral Charge Density
SOI	Silicon-On-Insulator
SPV	Saturation surface PhotoVoltage
TMA	Tri-Methyl-Aluminum
TMAH	Tetra-Methyl Ammonium Hydroxide
TOX	Top OXide
VB	Valence Band
VBT/VBM	Valence band Top / Valence Band Maxima
XPS	X-ray Photoelectron Spectroscopy

b

List of symbols

λ	Wavelenght
μ_e, μ_h	Electron, hole mobility
μ_B	Bohr magnetron
τ	Trap response time
ϕ_B	Bulk potential
φ_B	Angle between the magnetic field and the interface normal
ψ_S	Surface band bending
ω	Angular frequency
A	Area
B	Magnetic field (effective)
C_{ACC}	Accumulation capacitance
C_C	Capacitance corrected for R_S
C_{INS}	Gate insulator capacitance
C_{IT}	Capacitance contribution of interface traps
C_m	Measured capacitance
C_{OX}	Oxide capacitance
C_{Se}	Semiconductor capacitance
D_{IT}	Interface trap level density
E_a	Positron acceleration energy
E_C	Conduction band
E_F	Fermi level in the semiconductor
E_{FM}	Fermi level in the metal electrode
E_g	Band gap width
E_I	Intrinsic Fermi energy
E_{IT}	Energy level of the interface trap
E_t	Trap energy depth
E_V	Valence band
G_C	Conductance corrected for R_S
G_m	Measured conductance
G_P	Parallel conductance
$h\upsilon$	Photon energy
I_d	Drain current
$k_{(....)}$	Dielectric constant of (....)
n_i	Intrinsic carrier concentration
N_A	Acceptor concentration
N_{IT}	Concentration of interface traps
p	Free hole concentration
$p_{\mu r}$	Reflected microwave power
q	Elementary charge
Q	Charge
R_L	Load resistance
R_S	Series resistance
S	Doppler broadening lineshape parameter (central window)
$t_{high\text{-}k}$	Thickness of the high-k insulator
T	Temperature
T_{OX}	Oxide thickness
$T_{Si\ CAP}$	Silicon cap thickness
V_{FB}	Flat-band voltage
V_G	Gate voltage
V_{OX}	Voltage drop across the oxide
V_T	Threshold voltage
W	Doppler broadening lineshape parameter (wings)

Chapter 1

The evolution of semiconductor devices and the role of defects

The general public tends to be unaware of the exponential growth of information technology (IT). Being wired for linear thinking, we tend to overlook the simple evidence that the devices we carry in our pockets or use at work were simply science fiction just a decade ago. Yet, those who have been involved in the world of science and engineering recognize such (r)evolution under a simple name: Moore's law. When, while working for IBM in 1965, Gordon Moore noticed that the number of transistors (the leading element of IT) fabricated on a certain chip area tended to double in about every 2 years, he also gave to the scientific community a roadmap that unleashed the exponential trend that keeps shaping the world we live in.

Despite some adjustments to this roadmap, anyone can directly experience the reality of such progress, accomplished through countless innovative contributions. Any advance, from a better step in device fabrication to a more efficient design, can be considered as a brick added to the construction of what is nowadays universally recognized as the *Digital Revolution*. Nonetheless, looking more broadly at the evolution of microelectronic devices, the striking difference that comes forth when comparing the 1960s Jack Kilby's first integrated circuit with Intel's 486 processors that invaded western houses in the 90s, next with today's devices, mostly deals with in the physical dimensions of the transistors. From an overall size of the order of microns, devices today in production are approaching physical limits at atomic scale where literally few atoms are arranged in a proper configuration to achieve functionality.

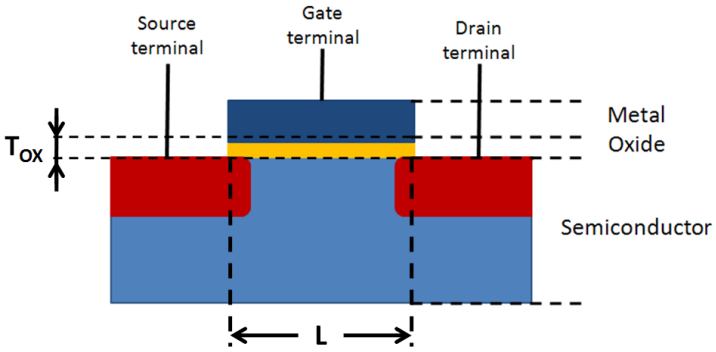


Figure 1.1: Schematic cross-section of the three-terminal MOSFET device. The critical node parameters, the channel length L, and the oxide insulator thickness T_{OX} are indicated. A device pursuing conduction through an electron-rich inversion channel (nMOSFET) is fabricated on a p-type substrate while a high concentration of donor impurities providing excess electrons (n-type doping) is introduced in the drain and source regions (red areas).

It is intriguing to see how such aggressive downscaling pushes progress towards the edges of the technological possibilities, where the "ideal" world in the mind of scientists and engineers has to face the truth of an imperfect reality, namely, **defects**.

1.1 CMOS technology

Device scaling and the era of disruptive innovations

Today's main actor on the stage of IT is still the Field Effect Transistor (FET), more specifically, the Metal-Oxide-Semiconductor FET (MOSFET).

Briefly, this transistor represents a 3-terminals semiconducting device where operation of one of the terminals enables one to switch electrical conduction across the remaing two terminals. A field effect transistor achieves this goal by modulating the charge carrier density in the channel between the source and drain terminals by means of an electric field induced by a voltage applied to the gate. Such device is schematically presented in Fig. 1.1.

When a certain electric field is applied to the terminal denoted as "gate", electrons can be attracted to or repelled from the terminal depending on the orientation of the electric field. Thanks to the insulating properties of the oxide layer, the electrons would either accumulate near the semiconductor/oxide interface, or leave it depleted. These two conditions would determine whether or

not a conducting layer, or channel, is formed between the “source“ and “drain“ terminals, and thus also control whether or not conduction between them is allowed. Ultimately, these two conditions may be used to represent the “0“s and “1“s logic levels upon which computers operate. Notably, the technology employing MOSFETs is called Complementary-MOS (CMOS) technolgy, for it achieves computation by combining MOSFET devices of two kinds: one operating conduction through an electron rich channel (*n-type*) and another one employing the hole rich, *p-type* channel.[1]

Since the invention in 1958 by Kilby and Noyce, transistors in the form as depicted in Fig. 1.1 made exclusively use of silicon as semiconducting material and of SiO_2 as oxide insulator.[2] For about three decades of the IT evolution, physical “scaling" is what drove the evolution of electron devices. Ideally, reducing the gate length L generally implies a faster device, while a smaller oxide insulator thickness , T_{OX}, translates into a larger insulator capacitance which implies a more controllable device and this, in turn, allows for reducing the applied supply voltage.

However, when the thickness of the oxide reaches the range of $\sim$ 1 - 2 nm, and the gate length approaches $\sim$ 50 nm, secondary effects begin to play a non-negligible role and any further reduction of physical dimensions introduces more drawbacks than advantages. On the one hand, for oxides thinner than 2 nm, each additional 0.2 nm reduction causes an increase of roughly one order of magnitude of gate leakage current [1]. This affects the ability to control the channel formation and increases the device power consumption. On the other hand, ever decreasing channel lenghts cause a deviation from the ideal MOSFET behavior -a feature that falls under the definition of “short channel effects"- primarily caused by uncrontrolled source-to-drain tunneling. These and other parasitic effects put a physical limit on the practice of geometric scaling. As a result, the microelectronic industry has by now entered an era driven by what is generally denoted as “disruptive“’ innovations.

The 90 nm and 65 nm technological *nodes*[3] (years 2003 - 2006) were characterized by the introduction of the **Strain engineering**, where the Si channel was deformed, or strained, to enhance its properties. In particular, by applying “tensile“ strain to the channel the transport properties of electrons

[1] These two doping conditions are put in place by introducing impurity atoms, or dopants, within the channel. Depending of the atoms used -donors or acceptors- one can introduce an excess of electrons or holes in the semiconductor.

[2] It is worth mention that in the late 60s even the top metal contact, which employed aluminum (Al) for its good conduction properties, was replaced by a highly doped polycrystalline Si (poly-Si) able to offer enhanced thermodinamic stability and better resistance to electromigration.

[3] In the microelectronic industry, successive device generations, or “nodes", are categorized by the average half-pitch of a generic memory cell, that is half the distance between identical features of the device.

can be enhanced. Similarly, the application of "compressive" strain increases the hole mobility.

The year 2007 saw the introduction of the **high-k/metal gate** (HKMG) technology. By that time, gate insulators were fabricated using a native Si dioxide layer of a thickness $T_{OX} \approx 1$ nm and any further thickness downscaling would lead to unsustainable leakage current (i.e., at this scale electrons can flow across the gate oxide by quantum tunneling). High-k materials are insulators with a dielectric constant, "k", higher than that of SiO_2 ($k_{(SiO_2)} = 3.9$). Thanks to this property, one is able to obtain the same capacitance value, which ultimately determines the electrostatic control over the channel, for a physically much thicker insulator. A hafnium-based oxide hit the market with Intel's 45nm HKMG technology in 2008. As a reference, depending on its crystallographic phase, pure HfO_2 can reach dielectric constants of around 20, about 5 times that of of silica, which translates directly into a factor of 5 in the physical oxide thickness. Yet, other insulating films have been extensively studied and the research in the field is still intense. So, in order to fairily compare different insulating technologies, it is of common use to refer to the Equivalent Oxide Thickness (EOT):

$$EOT = t_{\text{high-k}} \frac{k_{SiO_2}}{k_{\text{high-k}}}, \tag{1.1}$$

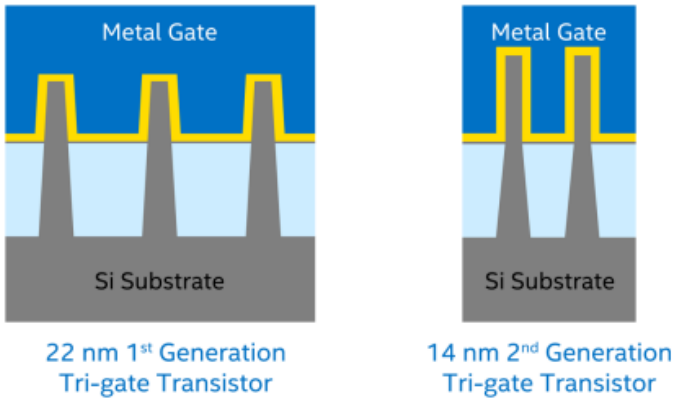
which indicates, for the same specific capacitance, how thick the insulator layer (or multi-layer) would have to be if made exclusively of SiO_2.

It has to be mentioned though that the transition to the HKMG technology entailed several challenges. For example, the deposition of a non-native oxide on Si was seen to cause oxidation of the Si surface, leading to the formation of a detrimental high-EOT Si-oxide interlayer (IL). Solution to this problem was later found in the **oxygen scavenging** process, where a reactive layer inside the gate electrode was used to consume the oxygen from the SiO_X interlayer, thus leaving behind an abrupt interface between Si and the HK material [2].

Also, despite the enhanced electrostatic control, the use of HK insulators was seen to correlate with a partial deterioration of the conducting properties of Si [3] [4]. In order to compensate for this partial loss in mobility, and further enhance the electrostatic control over the channel, in 2011 the **3D** technology was introduced. The first computer processor produced with such technology was commercialized by Intel in 2012 (the Ivy Bridge CPU).

Fig. 1.2 schematically shows the cross-section of the 1^{st} generation of 3D transistors, or Tri-gate transistors, fabricated by INTEL©for the 22 nm technology node, together with the 2^{nd} generation projected for the next 14 nm technolgy node.

It is interesting to notice, by comparing the schematics in Fig. 1.2



	22 nm Node	14 nm Node	Scale
Transistor Fin Pitch	60	42	.70x
Transistor Gate Pitch	90	70	.78x
Interconnect Pitch	80 nm	52 nm	.65x

Figure 1.2: Schematic cross-section of the 22 nm 1^{st} generation 3D FET and the projected 14 nm 2^{nd} generation FINFET. The table indicates the most notable dimentions of the structures: Fin, Gate and Interconnect pitch. The image has been retreived from INTEL©.com.

with the one presented in Fig. 1.1, how little of the original Kilby's 1968 integrated transistor has survived decades of progress. The only major feature still unchanged is the composition of the semiconducting channel, that is, silicon. In fact, whether exotic concepts such as tunnel-FETs and 2D heterostructures promise to offer much better performing devices in a more distant future, continuation of the trend described above will, in the coming years, rely on the replacement of Si with better conducting (high-mobility) materials.

In the next section, the main advantages and challenges involved with this transition from Si to high-mobility semiconductors are described.

1.2 Alternative channel materials

Ge and Ge-based alloys as replacement for Si

When a MOS transistor is in conducting mode, the current that flows between the source and drain, I_d, is directly proportional to the carrier mobility μ:

$$I_d = \frac{\mu C_{INS}}{2} \frac{W}{L} (V_G - V_T)^2, \tag{1.2}$$

where C_{INS} is the value of the gate insulator capacitance, W and L are, respectively, the width and length of the conducting channel, and (V_G - V_T) represents the bias condition: V_G is the potential applied to the gate terminal and V_T is the threshold voltage at which the conducting channel starts to be formed. High-mobility materials, as their name suggests, potentially allow for an increase of I_d and device performances.

Table 1.1 lists the room temperature (300 K) properties of several semiconducting materials, as compared to the two main different "flavors" of Si, that only differ for their crystallographic orientation in the conducting Si channel (in this case [100] or [110]).

Table 1.1: Bulk electron and hole, μ_e and μ_h, mobilities and bandgap width, E_g, of some semiconductors at 300 K [5][6].

Material	μ_e (cm^2/V·s)	μ_h(cm^2/V·s)	E_g (eV)
[100]Si	1600	430	1.12
[110]Si	1250	900	1.12
$Si_{0.25}Ge_{0.75}$		750	0.80
Ge	3900	1900	0.66
GaAs	9200	400	1.42
InP	5000	200	1.35
InAs	40000	500	0.36

Notably, the mobility values vary dramatically depending on the type of charge carrier. This implies that a non-Si based CMOS technology might have to deal with the additional complication that more than one channel material needs to be combined on the same chip.

The only exception, specifically addressed in this work, are Ge and Ge-based alloys which score better than Si in both electron and hole mobilities. This implies that, potentially, Ge can deliver enhanced electrical performances in both *n*- and *p*-channel devices thus alleviating the need for combining dissimilar channel material (some examples can be found in [7][8][9]).

Another reason that makes Ge particularly interesting is its small band gap width E_g. As can be seen in Table 1.1, E_g(Ge) = 0.66 eV, about half

that of Si. This feature would make it possible to reduce the device power supply voltage as well as the overall power consumption (a successfull example is reported in Ref.[10]).

However, the transition from Si to a different channel material requires overcoming a plethora of technological challenges related to their different intrinsic properties. First, the production of large-size semiconductor wafers of a high-mobility material is hampered if the material has larger mass density. Next, the cost of producing a 4 inch Ge wafer is approximatly 5 times the production cost of a 12 inch Si wafer, and the figure further rises for III-V semiconductors [4]. For these reasons, high-mobility channel technologies will probably still remain embedded on a Si platform, where thin semiconducting device channels are epitaxially grown on Si substrate wafers.

Whereas the growth of alternative channel materials on Si represents a complex and diverse matter which deserves its own field of study, a significant advantage of Ge over other semiconducting compounds (namely, III-V alloys) in terms of integration with Si consists in the fact that selective growth of SiGe layers has been part of CMOS processing already for several years (SiGe layers are used as “stressors" to impose tensile strain on Si channels).

A large number of scientists have also thoroughly investigated the SiGe alloys intended for fabrication of p-channel devices [11][12][13][14][15][16], to be introduced in the CMOS processing flow together with the conventional Si n-type channel devices. In Table 1.1 is reported μ_{h} and the band gap of the $Si_{0.25}Ge_{0.75}$ alloy. Interestingly, the bandgap width of this alloy can be tuned by changing the alloy composition [17].

As a matter of fact recently, in July 2015, IBM announced the first test chip for the 7 nm node that includes a SiGe vertical channel technology (cf. Fig. 1.2), indicating the will of important market players to move into this direction.

Yet, even though one could foresee the microelectronic industry as moving towards a SiGe and, ultimately, a pure-Ge based technolgy, it is expected to face several considerable challenges. The next section contains a brief summary of these issues together with an overview of the possible solutions. A more detailed and exhaustive discussion on this topic can be found in Ref. [18].

1.3 Challenges for the use of Ge-based channel materials.

Looking back at Table 1.1, one needs to keep in mind that the indicated mobility values refer to the “bulk“ semiconductor properties. In reality, the

[4] Semiconducting alloys fabricated by combining elements from the third and fifth column of the periodic table.

effective charge carrier mobilities in the MOSFET channel (cf. Fig. 1.1) can be much smaller since the electron transport may be affected by scattering due to the presence of imperfections and defects in the region close to the semiconductor/insulator interface.[5]

Furthermore, the interface defects also impair the electrical stability of the devices by trapping charges and, therefore, lead to reliability degradation and reduced device lifetime. Simply put, *the presence of high densities of electrically active defects in Ge-based structures is still an unsolved and a not-fully understood issue*. Here we attempt to overview the major technological challenges associated with the introduction of Ge-based channels into MOS devices, as well as the most common approaches to solve them.

There are multiple sources of imperfections at the Ge/Oxide interface. First, it is well known that surface oxidation of Ge results in chemically unstable (i.e., water soluble) and highly defective sub-stochiometric oxide layers [19][20][21]. This issue appears to be relevant also to SiGe alloys [22].

Next, since the Ge melting point is much lower than that of Si (938 $^{\circ}C$ versus 1412 $^{\circ}C$ for Si), this poses strict limitations on the processing temperature. Furthermore, widely aknowledged issues are related to the high diffusivity of Ge upon thermal treatment [23][24][25]. The impact of this diffusion phenomena depends on device structure and fabrication. For example, for the specific case of SiGe layers used to strain the channel in order to enhance carrier mobility, it has been found that Ge out-diffusion leads to layer relaxation, neutralizing the desired benefits [26]. Importantly, it has been predicted that the presence of Ge atoms in the high-k insulator on top will also cause additional threshold voltage instabilities [27].

With these considerations in mind, it does not comes as a surprise that surface passivation and interface engineering are the most compelling technological challenges for the realization of successful Ge-based MOS devices.

A review on technological advances in this field can be found in the literature[28][29]. Among the many strategies explored, one may identify four most promising approaches: (1) Ge surface nitridation; (2) Ge surface sulfurization; (3) Si-interlayer (IL) technology; (4) GeO_2 passivation. All these approaches have been associated with the potential to reduce the overall defectivity of the Ge/high-k stacks, but not always constitute a technologically feasible solution due to other limitations, such as not meeting the low-EOT ($<$ 1nm) requirement.

The surface nitridation represents one of the initial attempts to stabilize the interface region between Ge and the gate insulator, with succesfull

[5] As briefly mentioned in Section 1, when high-k metal-oxides are used, additional electron mobility degradation is also found due to remote phonon scattering (soft modes caused by the oscillation of the oxygen ions) [3]

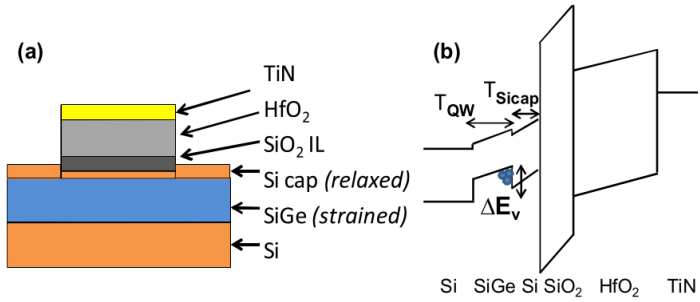


Figure 1.3: Schematic cross-section (a) and band structure (b) of Si-capped SiGe-channel pMOS devices fabricated at IMEC, as replotted from Ref. [35]. In (b) ΔE_V indicates the valence band offset between the Si and SiGe layers, giving rise to hole confinement (the *Quantum Well*, of thickness T_{QW}).

experiments dating back to the late 80's [30]. By annealing the oxidized Ge surfaces and interfaces in NH_3 ambient it has been repeatedly reported that electrical characteristics were improved as compared to un-annealed ones. This was ascribed to the formation of a more stable GeON IL between the substrate and the subsequently deposited high-k insulator [24] [31] [32].

Alongside the NH_3-treatment, sulfur passivation (sulfurization) has also been explored in the late 80's [33]. Later experimental and theoretical studies [34] indicate that exposure of the Ge surface to H_2S results in the formation of Ge-S-S-Ge bonds leading to a lower density of interface defects. Despite the better electrical performance, drawbacks of this approach are related to the incorporation of Ge in the gate insulator (see Ref. [31]) and the formation of an IL resulting in significant EOT penalty.

A more recent approach makes use of introducting a Si IL in between the Ge-based channel area and the high-k insulator on top. This technique aims at achieving the highest possible interface quality offered by the well controllable Si/SiO_2 interface, while still harvesting the gains offered by the high mobility of Ge and high-k insulating materials. An additional advantage of this technique comes from the final band structure of these multilayers. Fig. 1.3 shows a schematic cross section (a) and the band diamgram (b) of a Si-passivated SiGe-channel pMOSFET device fabricated at imec, Belgium. The concept of band structure of a MOS device will be explored in more detail in the next chapter. Nonetheless, the valence band top (VBT) discontinuity ΔE_V between the SiGe layer and the Si capping layer result in what is called a *Quantum Well* (QW) for holes. Its main effect is to confine holes within the SiGe channel region, physically separating them from the defective semiconductor/insulator

interface, and in this way attempting to attain a mobility closer to the bulk value. Importantly, a better reliability, as compared to the Si reference devices, was also reported on these devices [35]. Despite these advantages, there are problems related to the high Ge diffusivity. In particular, it was observed that even in Si-capped Ge devices, Ge atoms segregate at the surface of the Si IL during its deposition process [36], thus potentially contaminating the passivating stack and the gate insulator.

The last item on the list actually comprises different passivation strategies that share a common goal: If so far we have described different treatments aimed at avoiding the formation of a sub-stoichiometric GeO_x IL, the "last" approach, admitting its presence, aims at improving the overall chemical quality of this IL. One way to achieve this consists in the GeO_2 IL growth through low-temperature high-pressure thermal oxidation in molecular oxygen. It is believed that the latter improves the interface quality by avoiding the formation of interfacial dangling bonds and oxygen-deficiency defects. Indeed, better electrical performances have been reported by using this oxidation technique [37][38][39].

Another way of improving the electrical quality of the GeO_2 IL is based on the oxide doping with rare-earth metals. Thanks to their high polarizability, rare eath ions are believed to redistribute the electronic charge at the GeO_2/Ge interface, hence reducing the electrical activity of interface states which results in good passivating properties. In addition, rare earth oxides act as catalysts at the Ge surface favoring the formation of stable wide gap germanates over the unstable GeO_x species. Several succesfull attempts of using this approach have been reported in the literature [40][41].

All in all, as mentioned at the beginning of this section, interface defects not only reduce the charge carrier mobilities, but also undermine the reliability of the devices. This problem will be discussed in the next section.

1.4 Reliability issues in MOS devices

Bias Temperature Instability

The requirement to ensure sufficient reliability of electronic devices has a major impact on the process technology. As the CMOS technology evolved over the decades, the dominant failure mechanisms have also changed, eventually bringing to the attention a broad spectrum of physical phenomena.

For example, the aggressive geometrical scaling described in the previous sections was not accompanied by the corresponding lowering of the on-chip supply voltage, mostly because of the not improved sub-threshold slope of the MOSFET I_d-V_G characteristics. This has led to an increase of the electric field

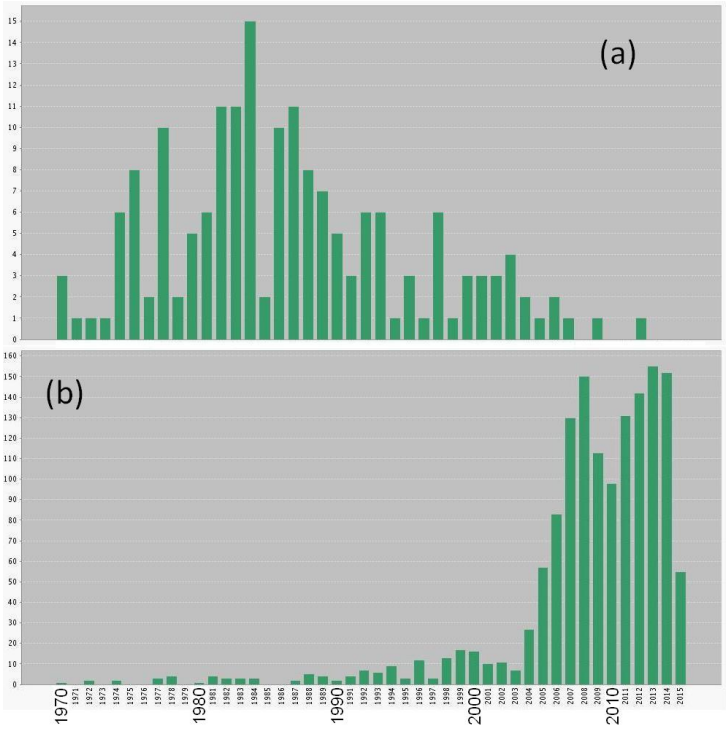


Figure 1.4: Citations reports, starting from year 1970, as listed by the Thompson Reuters Web of Science^{TM}. The first report (a) concerns citations in the fields “Ionic contamination" and “CMOS technology". The second report (b) corresponds to the search “Bias Temperature Instability" and “CMOS technology".

strength in the device, with oxide fields approaching dielectric breakdown limit of SiO_2 ($\sim$ 10 MV/cm) which, of course, threatens the transistor reliability.

In addition, many other degradation factors become relevant, eventually determining the final devices reliability. For example, while in the early days of the CMOS technology large attention has been devoted to ionic contamination of the gate oxide, this topic is rarely mentioned nowadays. By contrast, the Bias Temperature Instability - BTI, the main topic of this section - is gaining more and more interest. Fig. 1.4 plots the citation counts, starting from year 1970 and ending in 2015, for publications related to ionic contamination (a) versus BTI (b). It can be seen how BTI was of marginal concern before the year 2000. However, the mentioned high electric fields present in devices fabricated using

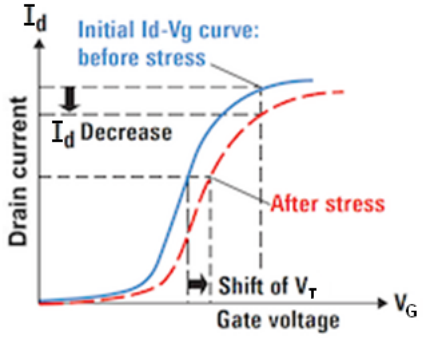


Figure 1.5: Schematic illustration of the effect of a positive bias and temperature stress on the MOSFET $I_{\mathrm{d}} - V_{\mathrm{G}}$ characteristic. The shift of the threshold voltage $\mathrm{V_T}$ and the reduction of the slope cause a reduction of the drive current flowing through the device. As replotted from Ref. [42]

more recent technology, together with the increase in the dissipated power, made the bias- and temperature- driven instabilities the primary factors impairing the device reliability.

The BTI phenomenon manifests itself as a shift of the threshold voltage of a transistor upon application of a certain voltage at elevated temperature [42] [43]. The magnitude of this shift correlates with the bias and temperature conditions imposed on the device, leading to the shift of the $\mathrm{I_d}$ - $\mathrm{V_G}$ curve accompanied by reduction of the sub-threshold slope. An example of such behavior in an n-type MOSFET is illustrated in Fig. 1.5 [42]. With increasing $\mathrm{V_G}$, the drain current, $\mathrm{I_d}$, increases due to the formation of the conducting (inversion) channel until saturation is achieved, corresponding to the maximum possible current between source and drain. Upon application of a positive bias at elevated temperature, a shift of the threshold voltage occurs together with a reduction of the I_{d} in saturation. This significantly affects all electrical parameters of the device and, importantly, may jeopardize the operation of extended circuitry, because the device-to-device threshold voltage variability becomes larger [44].

The origin of this behavior is trapping of additional charges within the MOSFET gate stack and the increase of the interface state density. For instance, for the case reported in Fig. 1.5, trapping of negative charges in the gate oxide and at its interface with the semiconductor channel necessitate application of a larger positive voltage to the gate electrode in order to accumulate the same density of electrons in the conducting inversion channel as compared to the

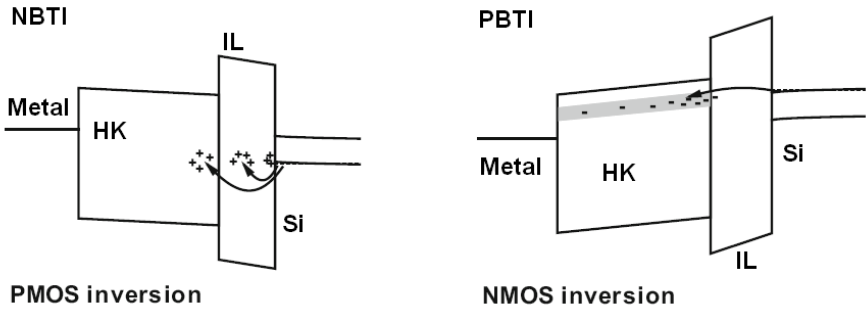


Figure 1.6: Schematic representation of the positive and negative charge trapping giving rise to N- and P-BTI degradation (replotted from Ref. [42]). IL stands for InterLayer, as the majority of the HKMG stacks intentionally include a buffer interlayer to passivate the semiconductor surface.

situation without these negative effects.

Fig. 1.6 illustrates this charge trapping behavior using the band diagrams of **Si** HKMG p- and n-MOS devices. The sign of the charges giving rise to the V_T shift depends on the polarity of the gate bias applied during the stress. For this reason the BTI phenomena are differentiated between negative BTI (NBTI), affecting p-channel MOSFETs, and positive BTI (PBTI) generally encountered in nMOSFETs.

The spatial location of the trapped charge was found to differ between PBTI and NBTI and this affects their impact on the transistor characteristics. For example, as illustrated in Fig. 1.6 for n-type Si HKMG transistors (PBTI), trapping of electrons occurs in the insulating oxide stack rather than at the channel/IL interface. As a consequence, the trapped charge is physically separated from the conducting channel and the carrier mobility is marginally affected. By contrast, NBTI (pMOSFETs) is thought to be caused by positive charge trapping in the region immediately adjacent to the semiconductor interface, thus causing additional Coulomb scattering in the channel and, therefore, impairing the mobility [45].

In some gate insulator stacks, the BTI-induced V_T shifts are seen to be partially recovered after the stress conditions are removed. For this reason one may identify two main BTI components: a *permanent* damage and a *recoverable* one. A more detailed study on the NBTI phenomena also indicated the permanent component to be caused by the generation of interface states during stress of the device, whereas the recoverable one was typically associated with charge trapping at pre-existing oxide defects [35].

It is thus becomes clear that *the understanding of the nature of charge trapping defects, their localization, their electrical characteristics and their dependence on device processing parameters is crucial to understand device reliability* [42]. Furthermore, significant differences in the BTI behavior of MOSFETs with Si and Ge channels [46] mandate specific attention to the role of the germanium-related charge traps.

1.5 Rationale of this work

The goal of this work is to contribute to the understanding of the physical nature of defects responsible for reliability degradation in Ge-based devices.

Several experimental techniques have been combined to obtain information concerning the atomic origin and electrical behavior of relevant defects. The identification of the nature of the defects giving rise to charge trapping can be achieved only by correlating the charge densities inferred from electrical measurements with data obtained through physical techniques. In the course of this work, the density of interface traps and their energy distribution D_{IT} (issue of the electrical activity of charge trapping centers) have been evaluated by using capacitance-voltage (CV) and conductance-voltage (GV) methods, as well as the Saturation surface PhotoVoltage (SPV) technique. Additionally, the spectral distribution of charge trapping centers present in the oxide insulators was studied by means of Exhaustive PhotoDepopulation Spectroscopy (EPDS). Physical analysis was carried out, when possible, by means of Electron Spin Resonance (ESR) and Positron Annihilation (PAS) spectroscopies. These techniques are described and discussed in the next **Chapter 2**.

Then, the thesis is organized as follows:

- In **Chapter 3** we address the defectivity of SiO_2/SiGe/SiO_2 heterostructures fabricated by the Ge condensation technique, a particularly advantageous method that allows the uniform growth of thin SiGe layers over a large wafer area. Importantly, the SiGe/SiO_2 interfaces in these devices are expected to be similar to the well characterized thermal Si/SiO_2 interface, allowing for a meaningful comparison. We will show how the density of the Ge dangling bond defects (DB), as well as the efficiency of the de-activation (passivation) process by hydrogen, correlate with the residual strain induced in the SiGe layer during its processing.
- Since the considerable lattice mismatch between Si and Ge makes strain hardly avoidable, the revealed impact of strain on the defectivity of the condensation-grown SiGe devices suggests new routes that may lead to the use of SiGe as channel material. In **Chapter 4** we report on the ESR

study performed on Si/SiGe/Si/HfO_2 structures as fabricated in Ref. [35] through epitaxial growth of a strained SiGe layer on Si substrate.

The results reveal the sole presence of Si DB interface centers, and show how reduction of the density of these defects, as compared to the reference Si-channel device, correlates with the presence of Ge in the channel region. Further analysis suggests that the interfacial defect density reduction is caused by out-diffusion of Ge atoms from the SiGe channel layer upon annealing.

- In **Chapter 5** the attention is turned to pure-Ge channel devices. In particular, by comparing interface trap densities at interfaces of Ge with different high-k insulators determined by means of conventional CV and GV methods with the results obtained through the SPV technique, we found that the majority of the charge trapping centers are located inside the oxide insulator. This trapping behavior differs significantly from that of silicon interfaces at which interface traps are largely associated with Si dangling bond defects.

- Finally, in **Chapter 6** the origin of the large defect density reported in Ge/high-k structures is addressed by studying oxide traps specifically. We found an additional contribution to the electron trapping in HfO_2 related to the presence of Ge contaminants within the oxide insulator. Their energy distribution, inferred using the EPDS technique, is found to align with the band gap of Ge, hence suggesting their direct contribution to the high D_{IT} found in Ge-based channel devices.

Bibliography

[1] Y. Taur, and E. Nowak *CMOS devices below 0.1 μm: how high will performance go?* IEEE Proc. IEDM '97, 215 (1997)

[2] H. Kim, P. McIntyre, C.O. Chui, K.C. Saraswat, and S. Stemmer *Engineering chemically abrupt high-k metal oxide/silicon interface using an oxygen-gettering metal overlayer* J. Appl. Phys., **96**(6), 3467 (2004)

[3] M.V. Fischetti, E. Cartier, and D. Neumayer *Reduction of the electron mobility in high-k MOS systems caused by remote scattering with interfacial optical phonons* Tech. Rep., **RC22734**, IBM Co. (2003)

[4] J. Robertson *High dielectric constant oxides* Eur. Phys. J. Appl. Phys., **28**, 265 (2004)

[5] http://www.ioffre.ru/SVA/NSM/Semicond/.

[6] S.M. Sze *Physics of semiconductor devices* (Wiley-Interscience, Hoboken, 1969)

[7] D. P. Brunco, B. De Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. Van Steenbergen, P. W. Mertens, M. Meuris, and M. M. Heyns *Germanium MOSFET Devices: Advances in Materials Understanding, Process Development, and Electrical Performance* J. of Electrochem. Soc., **155**(7), 552 (2008).

[8] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P.A. Pianetta, H.S. Wong, and K.C. Saraswat *High-mobility Ge N-MOSFETs and mobility degradation mechanisms* IEEE Trans. Electr. Dev., **58**(1), 59 (2011)

[9] P. Goley, and M.K. Hudait *Germanium based Field-Effect Transistors: Challenges and Opportunities* Materials, **7**, 2301 (2014)

[10] M.K. Hudait, M. Clavel, P. Goley, N. Jain, and Y. Zhu *Heterogeneous integration of epitaxial Ge on Si using AlAs/GaAs buffer architecture: Suitability for low-power Fin Field-Effect-Transistors* Nature Sci. Rep., **4**, 6964 (2014)

[11] L. Souriau, T. Nguyen, E. Augendre, R. Loo, V. Terzieva, M. Caymax, S. Cristoloveanu, M. Meuris, and W. Vandervorst *High-hole-mobility Silicon Germanium on Insulator substrates with high crystalline quality obtained by the germanium condensation technique* J. Electrochem. Soc., **156**(3), 208 (2009)

[12] S.G. Badcock, A.G. O'Neill, and E.G. Chester *Device and circuit performance of SiGe/Si MOSFETs* Solid-State Electron., **46**, 1925 (2002)

[13] A. Hikavyy, R. Loo, L. Witters, S. Takeoka, J. Geypen, B. Brijs, C. Merckling, M. Caymax, and J. Dekoster *SiGe SEG growth for buried channels p-MOS devices* ECS Meeting, **310**, 3001 (2008)

[14] G. Hellings, L. Witters, R. Krom, J. Mitard, A. Hikavyy, R.Loo, A. Schulze, G. Eneman, C. Kerner, J. Franco, T. Chiarella, S. Takeoka, W. Vandervorst, P. Absil, S. Biesemans, M. Heyns, K. De Meyer, M. Meuris, and T. Hoffmann *Implant-Free SiGe Quantum Well pFET: A novel, highly scalable and low thermal budget device, featuring raised source/drain and high-mobility channel* IEEE Proc. IEDM, 10.4.1 (2010)

[15] S. Verdonckt, E.F. Crabbc, B.S. Meyerson, D.L. Harame, P.J. Restle, J.M.C. Stork, and J.B. Johnson *SiGe-Channel Heterojunction p-MOSFET's* IEEE Trans. Electron Dev., **41**(I) (1994)

[16] D. Paul *Silicon germanium heterostructures in electronics: the present and the future* Thin Solid Films, **321**(1-2), 172 (1998)

[17] V.V. Afanas'ev, A. Stesmans, L. Souriau, R. Loo, M. Meuris *Valence band energy in confined $Si_{1-x}Ge_x$ ($0.28 < x < 0.93$) layers* Appl. Phys. Lett., **94**(17), 172106, (2009)

[18] C. Claeys and E. Simoen *Germanium-based technologies. From materials to devices* (Elsevier, Oxford, 2007)

[19] N. Taoka, W. Mizubayashi, Y. Morita, S. Migita, H. Ota, and S. Takagi *Nature of interface traps in Ge metal-insulator-semiconductor structures with GeO_2 interfacial layers* J. Appl. Phys., **109**, 084508 (2011)

[20] V.V. Afanas'ev, Y.G. Fedorenko, and A. Stesmans *Interface traps and dangling-bond defects in (100)Ge/HfO_2* Appl. Phys. Lett., **87**, 032107 (2005).

[21] K. Prabhakaran, and T. Ogino *Oxidation of Ge(100) and Ge(111) surfaces: an UPS and XPS study* Surf. Sci., **325**, 263 (1995)

[22] C.G. Ahn, H.S. Kang, Y.K. Kwon, S.M. Lee, B.R. Ryum, and B.K. Kang *Oxidation-induced traps near SiO_2/SiGe interface* J. Appl. Phys., **86**(3), 1542 (1999)

[23] N. Lu, W. Bai, A. Ramirez, C. Mouli, A. Ritenour, M.L. Lee, D. Antoniadis, and D.L. Kwong *Ge diffusion in Ge metal oxide semiconductor with chemical vapor deposition HfO_2 dielectric* Appl. Phys. Lett., **87**, 051922 (2005)

[24] S. Van Elshocht1, B. Brijs, M. Caymax, T. Conard, T. Chiarella, S. De Gendt, B. De Jaeger, S. Kubicek, M. Meuris, B. Onsia, O. Richard, I. Teerlinck, J. Van Steenbergen, C. Zhao, and M. Heyns *Deposition of HfO_2 on germanium and the impact of surface pretreatments* Appl. Phys. Lett., **85**(17), 3824 (2004)

[25] Q. Zhang, N. Wu, D.M.Y. Lai, Y. Nikolai, L.K. Bera, and C. Zhu *Germanium incorporation in HfO_2 dielectric on germanium substrate* J. Electrochem. Soc., **153**(3), 207 (2006)

[26] Y.S. Lim, J.Y. Lee, H.S. Kim, and D.W. Moon *Strain-induced anisotropic Ge diffusion in SiGe/Si superlattices* Appl. Phys. Lett., **80**(14), 2481 (2002)

[27] Q.Q. Sun, Y. Shi, L. Dong, H. Liu, S.J. Ding, and D.W. Zhang *Impact of germanium related defects on electrical performance of hafnium oxide* Appl. Phys. Lett., **92**, 102908 (2008)

[28] A. Toriumi, T. Tabata, C.H. Lee, T. Nishimura, K. Kita, and K. Nagashio *Opportunities and challenges for Ge CMOS - Control of interfacing field on Ge is a key* Microel. Engineering, **86**, 1571 (2009)

[29] Q. Xie, S. Deng, M. Schaekers, D. Lin, M. Caymax, A. Delabie, X. Qu, Y. Jiang, D. Deduytsche, and C. Detavernier *Germanium surface passivation and atomic layer deposition of high-k dielectrics - a tutorial review on Ge-based MOS capacitors* Semicond. Sci. Technol. **27**, 074012 (2012)

[30] J.J. Rosenberg, and Z.C. Martin *Self-aligned germanium MOSFET's using a nitrided native oxide gate insulator* IEEE Electron Dev. Lett., **9**(12), 639 (1988)

[31] N. Wu, Q. Zhang, C. Zhu, C.C. Yeo, S.J. Whang, D.S.H. Chan, M.F. Li, B.J. Cho, A. Chin, D.L. Kwong, A.Y. Du, C.H. Tung, and N. Balasubramanian *Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate* Appl. Phys. Lett., **84**(19), 3741 (2004)

[32] C.C. Cheng, C.H. Chien, G.L. Luo, C.H. Yang, M.L. Kuo, J.H. Lin, C.K. Tseng, and C.Y. Chang *Study of thermal stability of HfO_xN_y/Ge capacitors using postdeposition annealing and NH_3 plasma pretreatment* J. Electrochem. Soc., **157**(7), 155 (2007)

[33] K.T. Leung, L.J Terminello, Z. Hussain, X.S. Zhang, T. Hayashi, and D.A. Shirley *Surface-bonding geometry of (2 x 1)S/Ge(001) by the normal-emission angle-resolved photoemission extended-fine-structure technique* Phys. Rev. B, **38**(12), 8241 (1988)

[34] M. Houssa, G. Pourtois, B. Kaczer, B. De Jaeger, F.E. Leys, D. Nelis, K. Paredis, A. Vantomme, M. Caymax, M. Meuris, and M. Heyns *Experimental and theoretical study of Ge surface passivation* Microel. Engineering, **84**(9), 2267 (2007)

[35] J. Franco, B. Kaczer, P.J. Roussel, J. Mitard, M. Cho, L. Witters, T. Grasser, and G. Groeseneken *SiGe channel technology: Superior reliability toward ultra-thin EOT devices. Part I: NBTI* IEEE Trans. Electron Dev., **60**(1), (2013)

[36] B. Vincent, R. Loo, W. Vandervorst, J. Delmotte, B. Douhard, V.K. Valev, M. Vanbel, T. Verbiest ,J. Rip, B. Brijs, T. Conard, C. Claypool, S. Takeuchi, S. Zaima, J. Mitard, B. De Jaeger, J. Dekoster, and M. Caymax *Si passivation for Ge pMOSFETs: Impact of Si cap growth conditions* Solid-State Electron., **60**, 116 (2011)

[37] A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. Van Elshocht, M. Caymax, M. Heyns, and M. Meuris *Effective electrical passivation of Ge(100) for high-k gate dielectric layers using germanium oxide* Appl. Phys. Lett., **91**, 082904 (2007)

[38] F. Bellenger, M. Houssa, A. Delabie, V.V. Afanas'ev, T. Conard, M. Caymax, M. Meuris, K. De Meyer, and M. Heyns *Passivation of $Ge(100)/GeO_2$/high-k gate stacks using thermal oxide treatments* J. Electrochem. Soc., **155**(2), 33 (2008)

[39] C.H. Lee,T. Nishimura, K. Nagashio, and K. Kita *High-electron-mobility Ge/GeO_2 n-MOSFETs with two-step oxidation* IEEE Trans. Electron Dev., **58**(5), 1295 (2011)

[40] I.Z. Mitrovic, M. Althobaiti, A.D. Weerakkody, V.R. Dhanak, W.M.Linhart, T.D. Veal, N. Sedghi, S. Hall, P.R. Chalker, D. Tsoutsou, and A. Dimoulas *Ge interface engineering using ultra-thin La_2O_3 and Y_2O_3 films: A study into the effect of deposition temperature* J. Appl. Phys., **115**(11), 114102 (2014)

[41] C. Lu, C.H. Lee, W. Zhang, T. Nishimura, K. Nagashio, and A. Toriumi *Enhancement of thermal stability and water resistance in yttrium-doped GeO_2/Ge gate stack* Appl. Phys. Lett., **104**, 092909 (2014)

[42] T. Grasser *Bias Temperature Instability for devices and circuits* (Springer Science, NewYork, 2014)

[43] C. R. Helms, and E. H. Poindexter *The silicon-silicon dioxide system: Its microstructure and imperfections* Rep. Prog. Phys., **57**, 791 (1994)

[44] A. Asenov, S. Roy, R.A. Brown, G. Roy, C. Alexander, C. Riddet, C. Millar, B. Cheng, A. Martinez, N. Seoane, D. Reid, M.F. Bukhori, X. Wang, and U. Kovac *Advanced simulation of statistical variability and reliability in nano CMOS transistors* IEEE Proc. IEDM, 1.1.1 (2008)

[45] S. Pae, M. Agostinelli, M. Brazier, R. Chau, G. Dewey, T. Ghani, M. Hattendorf, J. Hicks, J. Kavalieros, K. Kuhn, J. Maiz, M. Metz, M. Mistry, C. Prasad, S. Ramey, A. Roskowski, J. Sandford, C. Thomas, C. Wiegand, and J. Wiedemer *BTI reliability of 45nm high-k metal gate process technology* IRPS, 352 (2008)

[46] J. Ma, W. Zhang, J.F. Zhang, B. Benbakti, Z. Ji, J. Mitard, J. Franco, B. Kaczer, and G. Groeseneken *NBTI of Ge pMOSFETs: Understanding defects and enabling lifetime prediction* IEEE Proc. IEDM, 34.2.1 (2014)

Chapter 2

Experimental techniques

> There are two possible outcomes: if the result confirms the hypothesis, then you've made a measurement. If the result is contrary to the hypothesis, then you've made a discovery
>
> E. Fermi

This chapter describes experimental techniques used in this work.

It is helpful to address first the differences between the two major types of characterization techniques, namely the electrical and the physical methods: Whereas electrical data can always offer a truthful insight on its own, it is only the correlation between the results obtained by complementary experiments that allows one to identify the atomic origin of charge trapping sites in semiconductor/insulator structures.

Electrical characterization techniques, as the name suggests, are based on the observation of electrical response of the devices. The first section of this chapter will specifically be focused on the **capacitance and admittance response** of the MOS structures. Two methods allowing one to evaluate the density of interface traps are described in detail, namely the **AC-conductance** and the **Grey-Brown** methods. As will further be discussed in Chapter 5, the abovementioned techniques, which were specifically developed around and tailored to the case of Si/SiO_2-based devices, frequently fail in addressing MOS structures fabricated on high-mobility semiconductors and high-k insulators. Thus, an alternative approach is proposed, which, as will be outlines, is based on the **Saturation surface Photovoltage** (SPV) measurements.

Next, in section 2.3, we will address trapping of charge carriers within the insulating layers. The energy distribution of trapped electrons is probed by the **Exhaustive PhotoDepopulation Spectroscopy** method introduced in this chapter.

Further, the physical characterization techniques will be described. First, we shortly overview the **Electron Spin Resonance** (ESR) spectroscopy. These experiments were performed by the group of Prof. André Stesmans. Finally, the physical background of the **Positron Annihilation Spectroscopy** (PAS) is presented in relation with defect analysis in semiconductor heterostructures.

2.1 Admittance response of an MOS structure

As briefly mentioned in the introductory chapter, an electrical potential applied to the gate terminal of a MOS structure changes the charge density in the semiconductor surface region. This, in turn, induces modulation of the band banding at the surface.

Fig. 2.1 shows the energy band diagram of an **ideal** p-type MOS capacitor under different external bias voltages (V_G). In this graph, E_C and E_V indicate the bottom edge of the semiconductor conduction band (CBB) and the top edge of the semiconductor valence band (VBT), respectively; E_I is the intrinsic Fermi level; E_F and E_{FM} are the Fermi energies (chemical potentials) in the bulk of the semiconductor and in the metal electrode, respectively [1].

Fig. 2.1(a) corresponds to the *flat-band* condition, in which no charge is present in the semiconducting layer and the effective work functions of semiconductor and metal electrodes are assumed to be equal. The gate voltage value at which this condition is reached is usually referred to as the flat-band voltage ($V_G = V_{FB} = 0$ in the shown ideal case). If the work functions of the MOS electrodes differ or, else, if a charge is present, $V_{FB} \neq 0$ may be observed. When a gate bias is applied, a certain band bending occurs in the semiconductor (denoted as qV_G and $q\psi_S$ in Fig. 2.1(b), respectively). Depending on the polarity and amplitude of the bias, three main conditions can be identified:

- *accumulation*, illustrated in Fig. 2.1(b), occurs when the majority carriers (in this case *holes*) are attracted to the semiconductor/insulator interface;
- *depletion*, shown in Fig. 2.1(c), occurs when the majority carriers are repelled from the interface and the Fermi level near the surface of the semiconductor is shifted towards midgap. Depletion occurs for gate biases between V_{FB} and the inversion threshold V_T. The latter is defined as the gate voltage at which the band bending potential ψ_S equals twice the bulk potential ϕ_B, i.e., $\psi_S = 2\phi_B = \frac{2}{q}(E_I - E_F)$.

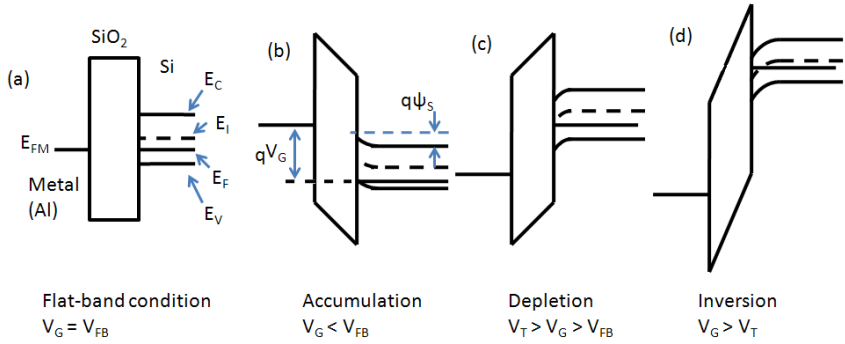


Figure 2.1: Band structure for a $p-type$ Si/SiO_2 MOS structure under various bias conditions: (a) flat-band, (b) accumulation, (c) depletion and (d) inversion

- *inversion*, Fig. 2.1(d), occurs when a gate voltage larger than V_T is able to induce an inversion layer in which concentration of minority carriers is larger than the majority carrier concentration in the bulk of the semiconductor.

The presence of charge trapping centers at the semiconductor/insulator interface, or within the oxide insulator itself, inevitably affects the electrical response of the device and alters the voltages at which the described conditions are attained. Importantly, the impact these defect states have on the MOS characteristics may vary significantly depending on the energy position of their levels and their electrical response time. As an example, we here refer to the well studied case of the Si/SiO_2 interface traps: The Si/SiO_2 interface charge trapping states are known to result from the presence of dangling bonds of Si atoms, whose physics and electrical behavior will be discussed more in detail in the next chapter. Depending on the trap ability to capture or to donate (release) an electron, this can be classified as an *acceptor* or *donor* trapping center, respectively. For acceptors, the trap levels are electrically neutral when empty and negatively charged when occupied by an electron. Conversely, donors are positively charged when empty, and neutral when occupied.

In the case of Si DBs, each physical defect may be in three charge states: positive (empty), neutral (single occupied), and negative (double occupied). This charge behavior gives rise to two distinct energy levels within the Si band gap, one which behaves as an acceptor and one as a donor (this makes the electrical behavior of the defect *amphoteric*). As llustrated in Fig. 2.2, the upper half of the Si band gap accomodates the acceptor levels, while the donor levels lie in the lower half of the gap (labelled with capital letter “A“ and “D“ in Fig. 2.2, respectively). At flatband condition (Fig. 2.2(a)), the donor states

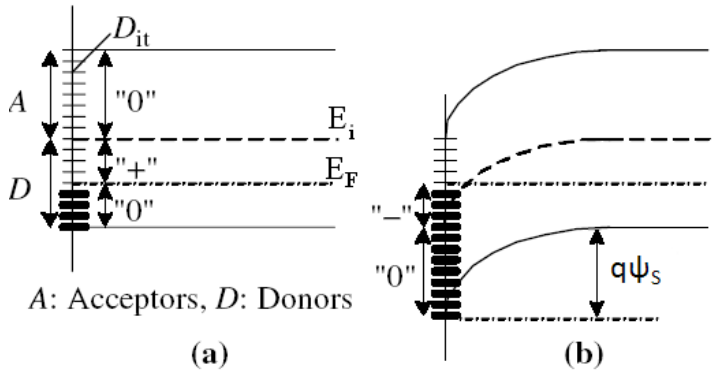


Figure 2.2: Band diagram for a p-type Si surface region containing the interface traps distribution typical of Si dangling bond defects, at flat-band conditions (a) and under the effect of a positive gate bias imposing a band bending $q\psi_S$ (b). The upper half of the Si band gap is populated by *acceptor* traps "A", whereas the lower half is populated by *donor* traps "D" [1].

below E_F in the p-type Si can be partially occupied by electrons and, hence, some of them will stay neutral (indicated as a "0"). The remaining donor states above E_F) are able to release their electron and become positively charged ("+"). At the same time all acceptor states in the upper half of the band gap remain empty and, therefore, neutral. When the bands are bent downwards under the effect of an external gate bias (Fig. 2.2(b)), all donor states are filled by electrons and, hence, become neutral. A fraction of the acceptor states (the ones below E_F) will be occupied by electrons and turn negative ("-").

As shown in Fig. 2.1, when MOS capacitor switches between accumulation and inversion conditions, the Fermi level is swept across the entire semiconductor band gap energy range. This implies that all the traps within this energy window are re-charged during the device operation, provided that the rate at which the Fermi level moves across the gap allows electron capture or emission from the trap.

If probing the electrical response in the frequency range close to the inverse capture or release time constants, the re-charging leaves a specific admittance signature inherent to the present interface traps. For this reason, probing the admittance response of MOS structures provides one of the most direct, and certainly the most used, ways to obtain information regarding the interface charge traps. In the next section this admittance spectroscopy is described for the ideal case, and the impact of charge trapping centers is

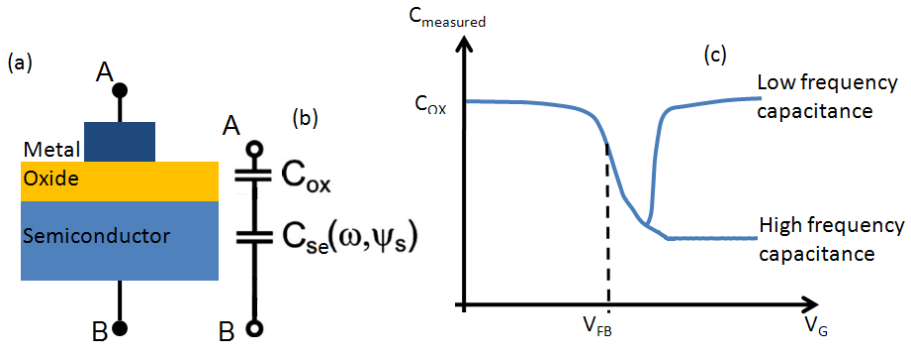


Figure 2.3: (a) Schematic of an ideal MOS structure and (b) its equivalent circuit; (c) High and low frequency CV curves for a generic p-type MOS structure.

discussed more in detail by presenting the AC-conductance and Grey-Brown methods of interface traps characterization in MOS structures.

2.1.1 CV and GV characterization

The charging and discharging of interface traps can be probed by analyzing the admittance measured across the MOS structure using an appropiate equivalent circuit (or model). Importantly, whereas in the previous paragraph we have described a *static* behavior of the MOS device, the **AC** characteristics provide by far more useful information.

In order to measure capacitance and conductance of an MOS capacitor as a function of gate bias, one applies a DC bias, which determines the E_F position at the surface of semiconductor corresponding to a certain surface potential ψ_S (see. Fig. 2.2(b)). This DC bias is superimposed with a small[1] AC signal inducing a frequency-dependent oscillation of ψ_S. The Capacitance- and Conductance-Voltage (CV and GV) curves are measured by slowly changing the DC bias (or changing it step-wise) while sweeping at the frequency of the modulating AC signal (typically in the range 100 Hz to 1 MHz in this work).

Fig. 2.3(a) shows the schematic cross-section of a **defect-free** MOS structure. Its equivalent circuit can be considered, in first approximation, as that depicted in Fig. 2.3(b), where C_{OX} represents the oxide capacitance and C_{se} the capacitance of the semiconductor surface layer. The latter contribution changes as a function of the band bending ψ_S and the frequency of the AC probing signal ω. It is important to mention that this equivalent circuit already

[1] The amplitude of the applied signal complies with the small-signal condition if it produces a linear response of AC current to AC voltage

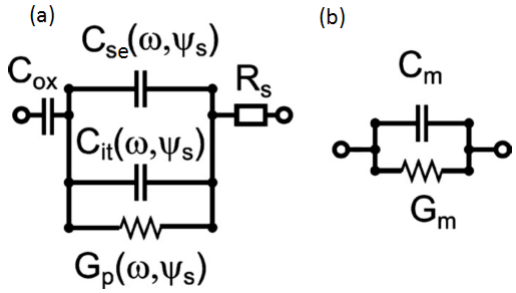


Figure 2.4: (a) Equivalent circuit of an MOS structure including the contribution of interface traps and series resistance and (b) equivalent circuit of the measured impedance. As replotted from [2].

embodies a number of assumptions and approximations (e.g. it does not take into consideration the series resistance).

Fig. 2.3(c) shows the high-frequency (HF) and low-frequency (LF) CV curves as they would be measured between terminals A and B assuming a p-type semiconductor. As can be seen, for $V_G < V_{FB}$ the majority carriers are accumulated at the semiconductor/insulator interface and the capacitance between terminals A and B approaches C_{OX}. When the semiconductor is in depletion ($V_G > V_{FB}$) the contribution of C_{se} is in series connection with C_{OX} and the overall capacitance becomes lower. By increasing further the gate bias V_G, two different trends occur depending on the frequency of the AC signal used. First, if the signal frequency is high enough for the minority carriers not to be able to respond, the overall capacitance reaches a minimum value given by the largest possible width of the depletion layer (for more details refer to Ref. [1]). Conversely, if the frequency of the AC signal is low enough to allow for the response from the generation/recombination of the minority carriers, the differential capacitance of the inversion layer will be high. As a result the overall capacitance measured between terminals A and B will again approach C_{OX}.

The presence of electrically active defects (charge traps) adds complexity to this scenario: traps with energy level within the range of ψ_S sweep can change their occupancy if the carrier trapping/emission time allows for it. Also, by including the effect of a series resistance R_S due to the resistivity of the bulk semiconductor and contacts, a more realistic equivalent circuit of the MOS structure can be proposed as shown in Fig. 2.4(a).

In this circuit, $C_{it}(\omega, \psi_S)$ and $G_P(\omega, \psi_S)$ represent the equivalent parallel

capacitance and conductance contributions originating from interface traps, and R_S is the series resistance. The admittance measured across an MOS structure can be described by the more simple equivalent circuit shown in Fig. 2.4(b). [2]

In order to determine C_{IT} and/or G_P, which represent quantities related to the interface traps parameters, experiments exploit the dependence of the equivalent circuit components on the AC frequency and surface potential (ω and ψ_S). A comprehensive review of the admittance-based methodologies developed in the past can be found in Engel-Herbert *et al.* [2]. In the next paragraph, the AC conductance method is described in more detail.

2.1.2 AC conductance method and solution of the Berglund integral

The application of the AC conductance method requires, as the first step, the reduction of the two equivalent circuits in Fig. 2.4 to an equal number of nodes. In order to achieve this goal, the measured C_m and G_m have to be corrected for the series resistance R_S.

When the MOS structure is biased in strong accumulation, the equivalent circuit can be assumed to contain only C_{OX} and R_S [1]. Hence, the series resistance can be inferred as follows:

$$R_S = \frac{G_{m,\,acc}}{{G_{m,\,acc}}^2 + \omega^2 {C_{m,\,acc}}^2} \quad . \tag{2.1}$$

Using this value computed per each probe frequency, the measured capacitance and conductance can be corrected as follows:

$$C_C = \frac{({G_m}^2 + \omega^2 {G_m}^2) C_m}{[G_m - ({G_m}^2 + \omega^2 {G_m}^2) R_S]^2 + \omega^2 {C_m}^2} \quad , \tag{2.2}$$

$$G_C = \frac{({G_m}^2 + \omega^2 {G_m}^2)[G_m - ({G_m}^2 + \omega^2 {G_m}^2) R_S]}{[G_m - ({G_m}^2 + \omega^2 {G_m}^2) R_S]^2 + \omega^2 {C_m}^2} \quad . \tag{2.3}$$

Once the contribution of the series resistance is eliminated, the conductance can be calculated from the corrected measured capacitance and conductance as follows:

$$G_P = \frac{\omega^2 {C_{OX}}^2 G_C}{{G_m}^2 + \omega^2 (C_{OX} - C_C)^2} \quad . \tag{2.4}$$

As already mentioned, interface traps with energy level close to the Fermi level can change their occupancy following the AC probing signal applied to the

[2] More specifically, this equivalent circuit corresponds to CV and GV measurements as performed by an LCR-bridge in the *parallel* mode. A series configuration is also provided by the instrument, but not used for our purposes.

gate electrode. This change in the charge state can be also seen as a loss of charge from the view point of the semiconductor. As a result, the electrical activity of the defects can be monitored by probing the measured conductance: recharging of an interface trap will be observed through a sudden increase in the measured conductance. Depending on the trap response time τ, the maximum conductance will be observed when the interface traps are in "resonance" with the AC signal [3]. Hence, by measuring the conductance across a broad range of frequencies, the trap response will lead to a peak of the (normalized) parallel conductance G_P at the frequency ω corresponding to the inverse trap time constant. Importantly, the height of these peaks is directly related to the density of interface traps responding to the AC signal at that specific frequency, given as:

$$D_{IT} \approx \frac{2.5}{Aq}(\frac{G_P}{w})_{max} \quad , \tag{2.5}$$

where A is the MOS capacitor area and q the elementary charge..

By using $G_P(\omega)$-ω plots measured at different gate voltages V_G, one is able to establish a relationship between specific interface traps and the surface potential ψ_S at which they respond. Determining the trap energy position within the semiconductor band gap thus requires an additional step, i.e., calculation of the band bending ψ_S induced by a given gate bias V_G. This is done by means of the **Berglund** method [3].

If using the equivalent circuit shown in Fig. 2.3(a), a bias V_G applied between the terminals A and B will be divided between the oxide layer and the semiconductor space charge layer. In equilibrium (low frequency condition, when the minority carriers and surface states can follow the AC signal), the slow changes in the applied voltage will be divided as follows:

$$\partial V_G = \partial V_{OX} + \partial \psi_S \quad . \tag{2.6}$$

The measured differential capacitance can be expressed as follows:

$$C_m = \frac{\partial Q_G}{\partial V_G} \quad . \tag{2.7}$$

The same charge change also corresponds to the voltage drop across the oxide insulator:

$$\partial Q_G = C_{OX} \partial V_{OX} \quad . \tag{2.8}$$

Therefore, Eq. (2.7) can be rewritten as:

$$C_m = C_{OX} \frac{\partial V_{OX}}{\partial V_G} \quad . \tag{2.9}$$

[3]This condition can be represented as $\omega\tau = 1$, where τ is the trap time constant, i.e., the trapping/emission time.

Next, combining Eq. (2.6) and Eq. (2.9) one obtains:

$$C_{\mathrm{m}} = C_{\mathrm{OX}} \left[1 - \frac{\partial \psi_{\mathrm{S}}}{\partial V_{\mathrm{G}}} \right] \quad , \tag{2.10}$$

and

$$\frac{\partial \psi_{\mathrm{S}}}{\partial V_{\mathrm{G}}} = 1 - \frac{C_{\mathrm{m}}}{C_{\mathrm{OX}}} \quad . \tag{2.11}$$

The latter expression can be numerically integrated to obtain the ψ_{S} value corresponding to the given $\mathrm{V_G}$ change: Defining $(1 - \frac{C_{\mathrm{m}}}{C_{\mathrm{OX}}}) = \alpha$, we obtain:

$$\psi_{\mathrm{n+1}} = \psi_{\mathrm{n}} + \frac{\alpha_{\mathrm{n+1}} + \alpha_{\mathrm{n}}}{2} + \Delta V_{\mathrm{G}} \quad , \tag{2.12}$$

where ΔV_{G} is the gate voltage step used to sweep $\mathrm{V_G}$ in measuring the CV curve.

Assuming that the CV curve complies with the LF condition, the $\psi_{\mathrm{S}}(V_{\mathrm{G}})$ relationship can be numerically computed by using Eq. 2.12 from the measured CV curve by providing, as boundary condition, a starting point ${\psi_{\mathrm{S}}}^0$. To do so, we proceed iteratively by assigning the starting value ${\psi_{\mathrm{S}}}^0$ for which the band bending at the flat band point is zero ${\psi_{\mathrm{S}}}^{FB} = 0$. This requirement implies accurate knowledge of the $\mathrm{V_{FB}}$. If assuming that the band bending lateral fluctuations are negligible, $\mathrm{V_{FB}}$ can be estimated according to the Schottky theory [1] from the intercept of the $\frac{1}{{C_{\mathrm{Se}}}^2} - V_{\mathrm{G}}$ dependence (where $\mathrm{C_{Se}}$ is the capacitance of the semiconductor) in the depletion range with the voltage axis.

Up to date, the AC conductance method is considered to deliver the most accurate estimate of the interface state density energy distribution $\mathrm{D_{IT}}(\psi_{\mathrm{S}})$. However, it provides no information regarding the atomic origin of the traps. Direct comparison of the electrical results to other atomically sensitive methods, like ESR (paramagnetic) spectroscopy has to be performed. Importantly, this comparison would require an additional integration step, since the ESR spectroscopy probes the total defect density per unit interface area $\mathrm{N_{IT}}$ while electrical measurements yield the trap density per unit area per energy interval.

Integrating $\mathrm{D_{IT}}(\mathrm{E_{IT}})$ across the semiconductor band gap width may introduce additional errors. On one hand, it is often not possible to estimate the $\mathrm{D_{IT}}$ across the *entire* semiconductor band gap. On the other hand, numerical integration of the Berglund integral is itself only an approximate solution. For this reason, other techniques may also be considered to estimate directly the $\mathrm{N_{IT}}$, in order to exclude some of the computational steps and reduce the final error. One of the techniques able to efficiently achieve this goal is the low-temperature CV analysis.

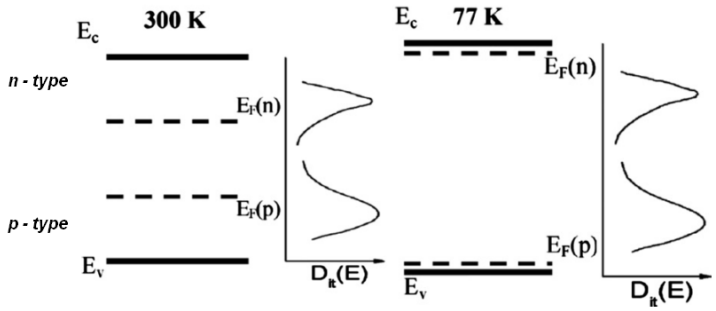


Figure 2.5: Temperature induced Fermi level shift with respect to the SiDBs energy distributions. As replotted from [6]

2.1.3 Gray-Brown method

The N_{IT} characterization method proposed by Gray and Brown in the late '60s [4] [5] specifically exploits the change in the defect charge state caused by the temperature-induced shift of the Fermi energy E_F relative to the trap energy level as illustrated in Fig. 2.2. In a p-type semiconductor, the Fermi level at equilibrium is determined as follows :

$$E_{\mathrm{F}} = E_{\mathrm{V}} + \frac{E_{\mathrm{g}}}{2} - \frac{kT}{q} \ln \frac{N_{\mathrm{A}}}{n_{\mathrm{i}}} \quad , \tag{2.13}$$

where n_i represents the *intrinsic* carrier concentration, N_A the acceptor concentration, and T is the absolute semiconductor temperature.

By lowering the temperature of the sample from $T_{(1)}$ to $T_{(2)}$ one induces a shift of the Fermi level towards the VBT. The situation is mirrored for *n-type* semiconductor, where temperature lowering will shift E_F towards the CBB. Fig. 2.5 illustrates the case for n- and p-type Si/SiO_2 interfaces in which two peaks in the D_{IT} energy distributions reflect the case of Si DBs interface traps (as replotted from [6]). As the temperature is lowered, all the defects found in between the two positions of E_F, at $T_{(1)}$ and $T_{(2)}$, will change their charge state. As a result, the gate bias V_{FB} required to establish the flat-band condition will also differ. The temperature-induced V_{FB} change is commonly referred to as the Gray-Brown shift:

$$V_{\mathrm{FB}}(T_1) - V_{\mathrm{FB}}(T_2) = -\frac{q \int_{E_{\mathrm{F}}(T_1)}^{E_{\mathrm{F}}(T_2)} D_{\mathrm{IT}}(E) dE}{C_{\mathrm{OX}}} \quad . \tag{2.14}$$

The interface traps density in the energy interval $\Delta E_{\mathrm{F}} = [E_{\mathrm{F}}(T_1), E_{\mathrm{F}}(T_2)]$ can then be calculated as:

$$\Delta N_{\mathrm{IT}} = \frac{(\Delta V_{\mathrm{FB}} - \frac{\Delta E_{\mathrm{F}}}{q}) C_{\mathrm{OX}}}{q} \quad , \tag{2.15}$$

where ΔV_{FB} is the Gray-Brown shift of the flat band voltage and ΔE_{F} is the temperature-induced shift of the Fermi level, as given by Eq. (2.13).

Next, since the Fermi energy at 77K is always very close to the band gap edges (< 20 meV), the $\mathrm{V_{FB}}$ difference between *p-* and *n-type* samples, at 77K will cover almost the entire semiconductor band gap, particularly taking into account the semiconductor gap widening at low T. Then, as reported by Thoan *et al.* [7]:

$$V_{\mathrm{FB}}(n) - V_{\mathrm{FB}}(p) = \frac{1}{q}(E_{\mathrm{F}}(n)) - \frac{1}{q}(E_{\mathrm{F}}(p)) + \frac{qN_{\mathrm{IT}}}{C_{\mathrm{OX}}} \cong E_{\mathrm{g}} + \frac{qN_{\mathrm{IT}}}{C_{\mathrm{OX}}} \quad . \tag{2.16}$$

The obtained $\mathrm{N_{IT}}$ value corresponds to all traps with energy levels distributed over the entire semiconductor band gap. Note that no surface potential determination is required in this method to obtain the total trap density.

2.2 Saturation surface PhotoVoltage

In this section we describe the Saturation surface PhotoVoltage (SPV) technique for interface traps characterization.

This method has been first proposed in the early 70s [8][9][11] to directly measure the semiconductor surface potential ψ_{S} at any given gate bias $\mathrm{V_G}$ since the SPV value directy corresponds to the variation of the band bending caused by high-intensity illumination. The distribution of interface trap density is then inferred with little additional computation from the difference between the measured $\psi_{\mathrm{S}}(V_{\mathrm{G}})$ relationship and the ideal curve corresponding to the defect-free MOS capacitor.

The principle of the SPV technique lies in the measurement of the illumination-induced change in the semiconductor surface band bending: When the surface of a semiconductor is illuminated by a light pulse, the generated electron-hole pairs cause reduction of the semiconductor band bending. This reduction defines the photovoltage (PV) value. If the light intensity is high enough to flatten the bands, the PV signal reaches the saturation value, which exactly corresponds to the initial surface potential value in darkness ψ_{S}. Thus, by measuring the saturation PV, one may directly determine the semiconductor band bending for any given DC bias $\mathrm{V_G}$ applied to the MOS capacitor. Noteworthy is that in saturation the *flat band state is insensitive to*

the presence or occupancy of interface traps [14]. Therefore, the zero PV always corresponds to $V_G = V_{FB}$.

Once the relationship between the band bending and the gate voltage is established, the defect contribution can be calculated using the Terman's model [12]: By sweeping the DC gate voltage slowly enough (quasi-static measurement), the surface potential measured through SPV will reflect the re-charging of interface traps, the density of which is then calculated as:

$$D_{IT}(\psi_S) = \left[\frac{C_{OX}}{q}[(\frac{d\psi_S}{dV_G})^{-1} - 1\right] - \frac{C_S}{q} \quad , \tag{2.17}$$

where C_{OX} is the capacitance of the insulating stack, $\frac{d\psi_S}{dV_G}$ is the slope of the band bending-gate voltage relationship as probed by the SPV measurements, and $C_S(\psi_S)$ is the semiconductor capacitance, computed assuming a uniform in-depth doping profile.

Importantly, whereas the AC-conductance method described before senses only traps with a response frequency within the range 100 Hz - 1 MHz (corresponding to a response time between 0.01 sec and 1 μsec), the SPV technique potentially allows the characterization of **all** traps, regardless of their time constant since they will be allowed to re-charge between light pulses with time constant 1 - 10 sec. This feature will be explored more in detail in Chapter 5. Next, the experimental set-up and the measurement procedure are described.

2.2.1 Experimental set-up

In the past, one of the main limitations that hindered the wide use of the SPV technique have been related with the availability of light sources of sufficient intensity. Recently, such lamps have been commercialized and, in our case, the set-up employs a Heraeus Xe flash lamp (type FXE5B) producing high intensity light pulses (2 J max energy per $\approx 100\mu sec$ long pulse). This was combined with low-pass filter/focusing optics (light wavelenght $\lambda > 360nm$) to avoid electron-hole pair generation in the insulating oxide, which would otherwise cause charge trapping upon illumination.

Fig. 2.6(a) illustrates the schematics of the experimental set-up: The PV was sensed on a load resistor R_L in series connection with the MOS sample under investigation. The load resistor value was selected ($R_L = 40k\Omega - 5.6M\Omega$) according to the sample capacitance so that the resulting time constant RC_{ACC} (C_{ACC} is the capacitance of the sample biased in accumulation) is always larger than the light pulse time width. This long time constant prevents charge loss during measurement, so that the whole PV signal will appear on R_L without interference with the electromagnetic pulse caused by the light source [8][9].

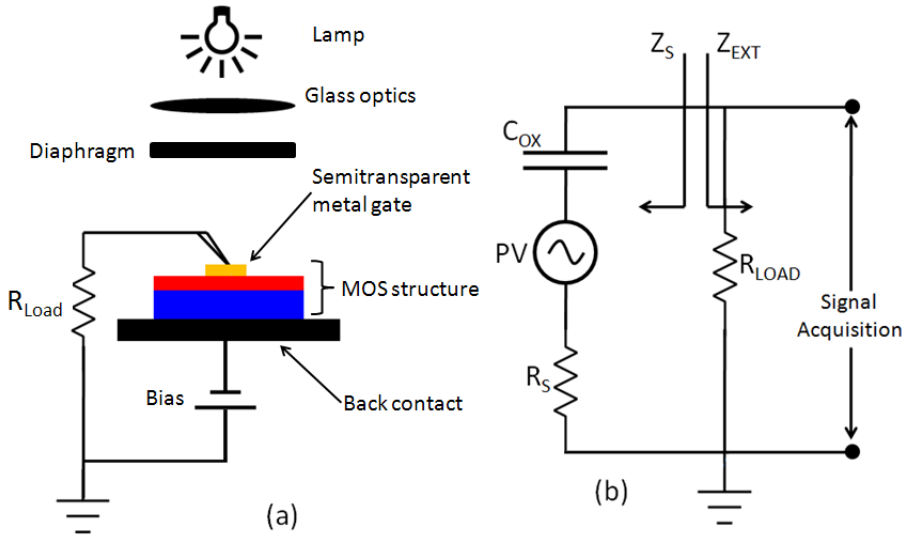


Figure 2.6: (a) Schematic of the SPV experimental set up and (b) simplified equivalent circuit.

This condition was described in more formal terms by Kronik *et al.* [10]. By assuming that the signal acquisition occurs through an infinite resistance and that the bias is applied through a negligible one, the experimental set-up equivalent circuit can be represented as shown in Fig. 2.6(b). There, C_{OX} represents the capacitance of the sample insulator and R_S its series resistance. When sensing the surface PV in a MOS structure the (external) measured signal approaches the actual change in the semiconductor band bending if $Z_{ext} >> Z_S$, i.e., if the external impedance seen by the sample (Z_{ext}) is much larger than the internal impedance of the sample itself (Z_S). This mandates the use of a sufficiently large R_{Load}.

Once the appropriate load resistor is chosen, PV transients are measured on the sample, biased in accumulation or depletion, as a function of the light intensity using an iris diaphragm to attenuate the light intensity. Saturation of the maximum value of these transients indicates that the light absorbed by the sample is sufficient to flatten the bands.

To illustrate this procedure, Fig. 2.7(a) shows the maximum value of voltage transients measured on a control (100)Si/31 nm SiO_2/Au hydrogen passivated sample, at bias conditions of accumulation and inversion, as function of the diaphragm aperture position. Here position "0" corresponds to the diaphragm completely shut, and position "6" to the maximum aperture. In Fig.

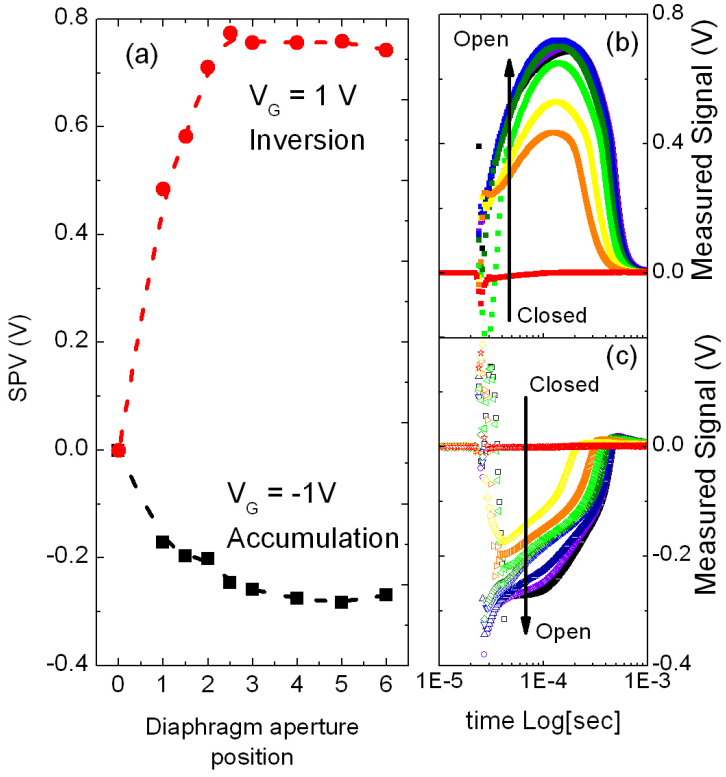


Figure 2.7: (a) SPV values, defined as the maximum value reached by the transient signal, as measured on the p-type (100)Si/31 nm SiO_2/Au reference sample as a function of the aperture position of the diaphragm interposed between the sample and the lamp. Position "0" corresponds to diaphragm closed, position "6"corresponds to diaphragm completely open. Measured signals, for different diaphragm aperture positions, at bias conditions of (b) inversion (V_G = +2V) and (c) accumulation (V_G = -1V) are shown for comparison.

2.7(b) and (c) the full signal transients are shown. The signal readout was set to be triggered by the falling edge of the electrical pulse generated to trigger the Xe flash lamp. It can be seen that the maximum constant value of the measured PV signals is already reached for the diaphragm aperture at about position 2, thus affirming that the saturation condition is attained. Finally, one can define as **SPV** value, corresponding to the total band bending, *the maximum value reached by the measured signal*. Importantly, the spread in these saturation values (in this case ≈ 0.05 V) gives an estimate of the measurement accuracy.

When recording the whole PV - V_G dependence, a time lapse of 3 seconds between consecutive light pulses was chosen in order to guarantee relaxation of the sample to the equilibrium state in darkness and avoid over-heating. In this way, we were able to detect charging of traps with characteristic time constant ≤ 3 s.

Surprisingly, whereas the SPV technique has been applied to the conventional Si-based capacitors in the past [8][9][10], high-mobility substrate devices with high-k insulators have escaped this analysis so far. In particular, as indicated by the authors cited above (in particular Ref. [10]), two main issues might be a reason of concern. First, novel high-mobility channel devices are typically fabricated as multi-layered structures (often on Si as carrier wafer). Therefore, the presence of additional interfaces buried beneath the semiconductor surface layer might affect the PV measurements. Another issue specifically concerns the application of the SPV characterization method to III-V semiconductor interfaces, and arises from the possible development of the Dember potential. This photo-voltage component is due to the different diffusion length of electrons and holes in the bulk semiconductor, and leads to the development of an electric field (the Dember field) compensating this diffusivity differences. Since this PV component is proportional to the photo-generated charge carrier density, its influence can be revealed by observing the PV-intensity behavior at high excitation levels.

2.3 Exhaustive PhotoDepopulation Spectroscopy

The technique presented in this section has been developed at KULeuven and is used for characterization of the energy distribution of defects localized in the insulator. For the scope of this work, a dedicated set-up has been built.

The physical principle of the Exhaustive PhotoDepopulation Spectroscopy (EPDS) is based on the phenomenon of optically-induced depopulation of defect states with levels within the band gap. When a defect within an insulating layer is illuminated by light with photon energy sufficient to excite the trapped charge carrier to the band states, this defect can be ionized. Photoexcitation of charge carriers generates a photocurrent and leads to a variation of the fixed charge, which can be monitored by measuring the shift of

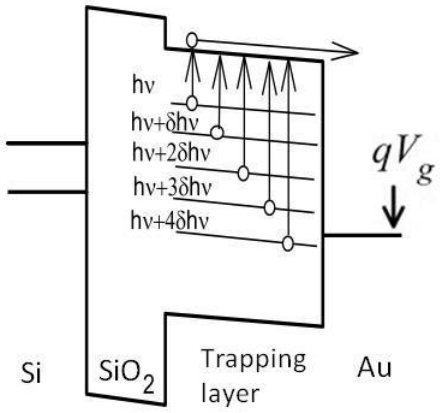


Figure 2.8: Schematic representation of electron transitions during the EPDS experiment on a Si/SiO_2/trapping layer/Au capacitor with increasing photon energy in steps of $\delta h\upsilon$.

the CV curves.

EPDS experiments are performed by stepwise increasing the energy of the illumination photons from $h\upsilon$ to $(h\upsilon + \delta h\upsilon)$, $(h\upsilon + 2\delta h\upsilon)$, etc. as illustrated in Fig. 2.8. During illumination, a positive gate bias (usually $V_G = 2$ V) is applied to the top metal electrode (in this case Au) in order to collect electrons released from the traps. Thanks to the saturation of the photoionization kinetics at each photon energy, the charge variation upon every increment $\delta h\upsilon$ directly corresponds to the density of gap states within the energy interval between the current and the previous $h\upsilon$ values. At the same time, the saturation charge value is not influenced by the *a priori* unknown defect photoionization cross-section [15].

Importantly, this technique also allows one to determine the type of charge trapping center. The comparison between results obtained on a pristine (un-charged) and an electron-injected sample allows one to assess densities of donor (0/+ transitions) and acceptor (-/0 transitions) states. Removal of electrons from donor states will lead to a negative (left-)shift of the CV curves measured after each illumination step, corresponding to generation of fixed positive charge [15]. On the other hand, the injection of electrons in the oxide insulator will populate, if present, acceptor traps and an additional negative oxide charge will be observed as a net positive (right-)shift of the CV curves. The photo-induced depopulation of these acceptors will successively remove these additional electrons, causing the CV curves to return to its pre-injection

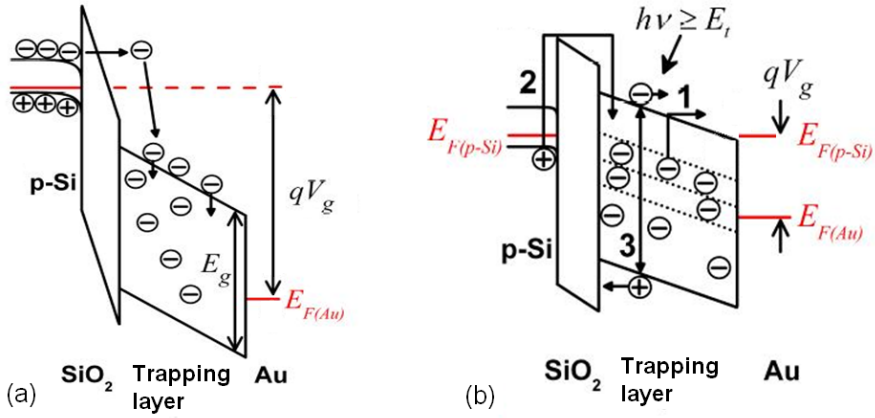


Figure 2.9: Band diagrams of a p-type Si/SiO_2/trapping layer/Au structure during (a) e^--injection from the Si substrate and (b) the different electron transitions occurring depending on the photon energy. The inclined dotted lines in (b) are intended to represent the $\delta h\upsilon = 0.2eV$ energy interval of the applied illumination. Courtesy of WanChih Wang [17]

position.

The validity of the proposed picture is based upon previous experiments performed on Al_2O_3 and HfO_2 layers [16], where no evidence was found for hole trapping in the bulk of these oxides. Removal of holes from the insulator would result in the observation of the (same amount of) negative charge, regardless of the orientation of the applied electric field. On the one side, when a positive gate voltage is applied during illumination, removed holes would drift and accumulate at the SiO_2/high-k interface. Internal Photo Emission (IPE) of electrons from silicon would compensate these carriers, leaving a net negative charge difference. On the other side, when a negative gate voltage is applied during illumination, removed holes would be collected at the metal electrode leaving the same negative charge difference as in the scenario described above. However, experiments performed by monitoring charge removal from the insulating layer at opposite field orientations did observe exclusively trapping or removal of charges, thus justifying to focus solely on the electron transitions.

The electron-injection in the insulating layer can be stimulated by applying a positive voltage pulse to the metal gate. If this voltage pulse has sufficient amplitude, it will cause electron tunnelling from the Si substrate through the SiO_2 barrier layer as shown in Fig. 2.9(a) for a p-type MOS device.

Several optically-induced electron transitions may cause oxide charge

variation, as illustrated in Fig. 2.9(b). First, traps can be depopulated when illuminating the sample with the photon energy ($h\upsilon$) increasing from 1.3 to 6.1 eV in steps of $\delta h\upsilon = 0.2eV$ (transition **no. 1** in Fig. 2.9(b)) [4]. In this way, the energy distribution of gap states in the trapping layer (defects of the oxide insulator) can be determined until the limit set by the energy threshold of IPE from silicon. The latter transition, labeled as **no. 2** in Fig. 2.9(b), occurs when the photon energy is high enough to excite electrons from the semiconductor substrate VBT across the oxide layer barrier (for a Si substrate and SiO_2 tunneling layer this threshold is 4.25 eV). The photo-injected electrons may be trapped in the insulating stack, thus causing negative charging. The last transition, labeled as **no. 3** in Fig. 2.9(b), occurs when the photon energy becomes sufficient to generate electron-hole pairs in the insulator. In the experiments described in this work, the *PhotoConductivity* transitions lead to accumulation of positive charges due to holes drifting towards the Si/SiO_2 substrate [16].

Each Photodepopulation step was carried out for 45 min at each $h\upsilon$ in order to ensure saturation of the depopulation kinetics (removal of at least 90 % of trapped electrons). Samples subjected to electron injection were first kept in darkness for > 12 h to ensure the stability of the remaining oxide charge during the EPDS measurements.

The oxide charge was monitored using the flatband voltage shift ($\Delta V_{\mathrm{FB}}(h\upsilon)$) of the CV curve measured across the device at 200 kHz (high frequencies are needed to reduce the effect that interface traps might have on V_{FB}). From this shift the spectral charge density (SCD) can be calculated as

$$SCD = \frac{\Delta Q(h\upsilon)}{\delta h\upsilon \cdot q} = \frac{-2C \cdot \Delta V_{\mathrm{FB}}(h\upsilon)}{\delta h\upsilon \cdot q} \quad , \tag{2.18}$$

where $\Delta Q(h\upsilon)$ is the charge variation within the given $h\upsilon$ interval upon illumination and C is the specific insulator stack capacitance. The final accuracy on the extracted SCD depends on the error in measuring V_{FB} and the EOT of the trapping layer. More details on this characterization technique can be found in the literature [18].

2.4 Electron Spin Resonance

Electron Spin Resonance (ESR) spectroscopy is a physical characterization technique able to identify the atomic structure of defects. Importantly, it can also quantify the density of observed defects in absolute terms allowing,

[4] Removal of charges located within ≈ 1.3 eV of the CBB of the trapping layer probably occurs via field- or thermally-induced transitions

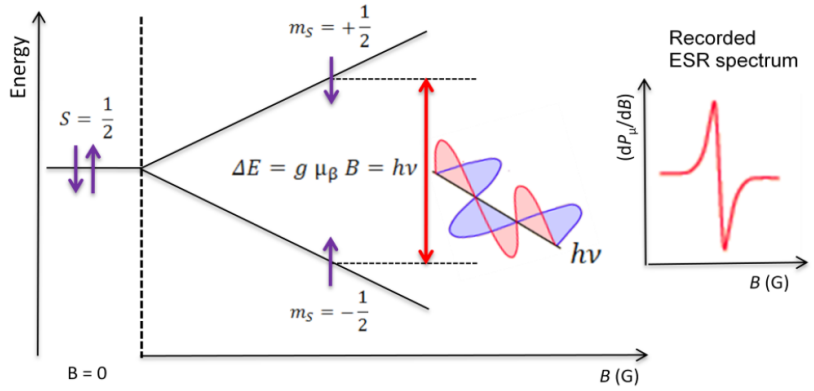


Figure 2.10: Representation of the Zeeman effect: the splitting of spin energy levels for an unpaired electron in an external magnetic field B. Absorption of a microwave photon can occur when its energy $h\nu$ matches the width of Zeeman-induced energy gap. ESR experiments routinely detect the first-derivative of the microwave absorption spectra. Courtesy of Jacek Kepa [19].

therefore, for quantitative correlation with the electrical response of interface or oxide charge traps.

This technique is based on observations made in 1896 by the Dutch physicist Peter Zeeman. He observed that the optical emission spectral lines, measured from different atoms, split when the sample is exposed to a magnetic field (Zeeman effect). This observation later led to the identification of the quantized angular momentum, or spin, of electrons and brought Zeeman the Nobel prize in physics in 1902.

Generally, an unpaired electron (e.g., a free electron, or unpaired electron residing at a defect in a solid) is characterized by a magnetic momentum $\bar{\mu} = g\mu_B\bar{S}$, where g is the spectroscopic splitting factor (simply referred to as the g-factor), $\mu_B = 9.274 \times 10^{-24} JT^{-1}$ the Bohr magneton, and S the spin angular momentum quantum number.

In an applied (external) magnetic field B the magnetic moment of an unpaired electron will be oriented either parallel (M_S = - $\frac{1}{2}$) or anti-parallel (M_S = + $\frac{1}{2}$) to the field, leading to an energy splitting between spin-up and spin-down states, as illustrated in Fig. 2.10. The Zeeman splitting between these two energy levels reflects the energy needed to flip the electron spin.

Electrons can be turned between the two energy levels by absorbing (or releasing) a photon. ESR experiments make use of the Zeeman principle to induce spin transitions between the Zeeman levels (M_S = - $\frac{1}{2}$ → + $\frac{1}{2}$) through

resonant absorption of microwave photons (commonly $\sim$ 9 GHz - 35 GHz range). Thus, a net absorpion of energy will be observed when the photon energy $h\upsilon$ matches the Zeeman-induced energy gap ΔE:

$$\Delta E = h\upsilon = g\mu_{\mathrm{B}}B \qquad . \tag{2.19}$$

As described in Eq. 2.19, the splitting between the two Zeeman energy levels is proportional to the Borh's magneton, the *effective* magnetic field B (which accounts for both the external and the local magnetic fields) and the **g-value**.

Since the g-value is sensitive to the wave function of the electron, analysis of the ESR results, e. g., using the first-derivative of the absorption spectra as shown in Fig. 2.10, may potentially be used to identify paramagnetic defects. In this way, ESR has been applied to the study of defects in Si/SiO_2 structures since the late '70s [20][21].

The intensity of ESR signal is directly related to the total number of un-paired spins. Therefore, once a defect is identified by isolating the corresponding ESR signal, the density of paramagnetic defects can be determined by using double numerical integration of the experimentally observed absorption-derivative spectra.

In the realization of this work, the ESR spectrometry was provided by the group of Prof. André Stesmans, hence we refer to the literature for more details [22].

2.5 Positron Annihilation Spectroscopy

Positron Annihilation Spectroscopy (PAS) represents a family of non-destructive spectroscopic techniques used, among others, for the studies of vacancy defects in solids [23].

The *positron* (e^+) is the **anti**particle of the electron (e^-). These two particles have approximately the same mass, the same spin, but opposite charge and magnetic moment. Positrons are stable in vacuum, however, when thermalized [5] in solids they react with the electrons in an annihilation reaction that produces γ-radiation:

$$e^+ + e^- \rightarrow 2\gamma \qquad . \tag{2.20}$$

This radiation is composed by 2 γ-photons ($h\upsilon$ = 511 keV) emitted collinearly in opposite directions (at an angle of 180°) and contains information about the electron density and atomic structure of the environment in which the annihilation reaction takes place. PAS probes different aspects of this

[5] *Thermalization* means the particle being in thermal equilibrium with the sample.

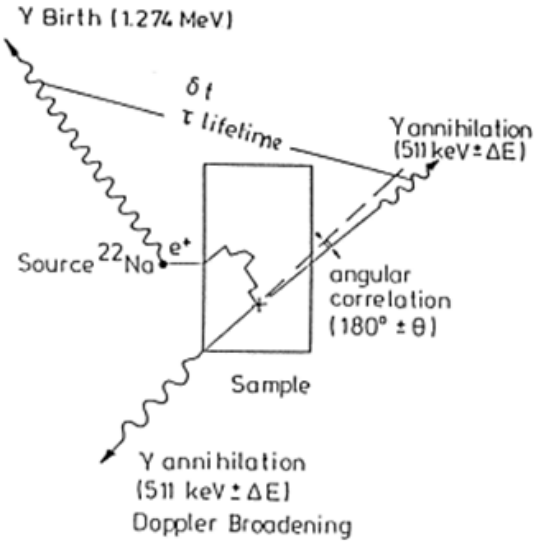


Figure 2.11: Illustration of the principles of the Positron Annihilation Spectroscopy. The e^+ - e^- annihilation events emits two γ-ray photons in opposite directions.

radiation to reveal characteristics and features of the atomic environment of the annihilation site.

A schematic of the PAS experiment is illustrated in Fig. 2.11, indicating three main modes for PA spectroscopy:

- Measurements of the positron e^+ lifetime address the time difference between photons originally emitted by the radioactive decay of the positrons source, and the annihilation photons. Trapping of positrons on defects can be evidenced by large delays.
- Angular correlation analysis is based on probing the additional, as compared to the ideal 180° degrees, angular deviation of the two photons produced by the annihilation event. Conservation of angular momentum implies that information regarding the annihilation environment is conserved and included in this angle.
- The Doppler broadening (Db) mode probes the additional energy, as compared to the ideal 511 keV, of the photons produced by each annihilation event. Since this method has been used in the present work, it will be discussed in more detail below.

The choice of the Db mode was dictated by the ability to sense defects in thin layers and interfaces by making use of slow, monoenergetic positron beams.

After being generated by a Na^{22} source, positrons are moderated by directing their beam through a thin (3 μm thick) 99.95 % pure polycrystalline tungsten foil in transmission geometry. The beam is subsequently pre-accelerated to 115 eV and transported to a 10 mT static axial magnetic field energy separator, formed by a set of coils in Helmholtz configuration, which allows a bent tube of 1 m curvature radius to filter out fast positrons. Next, the beam is accelerated and directed towards the sample with tunable energy (0 to 30 keV). Depending on the used set up, the final positron beam has a diameter of about 8 nm and and an intensity flux of about $10^5 e^+ cm^{-2} sec^{-1}$. After implantation in the sample, positrons need a few picoseconds to thermalize. Next, three main scenarios may be followed: First, e^+ can remain de-localized (so called Bloch state) and diffuse inside the sample until annihilation occurs. In low-defect monocrystalline materials, most of the annihilation events occur via this mechanism. Second, e^+ can get trapped on a defect. As a result, the positron wave-function becomes localized until annihilation occurs. Finally, positrons can diffuse towards the sample surface, where they can be trapped at a surface state or even be re-emitted into vacuum.

Spectroscopic analysis of a pure $e^+ - e^-$ annihilation will result in a single straight line exactly at the energy of 511 keV. However, since the (non-zero) momentum of the electron-positron pair is conserved in the annihilation event, there is an additional energy contribution which broadens the 511 keV photon energy line. Fig. 2.12 shows an example of the spectral distribution of annihilation events characterized by a non-negligible Doppler broadening. As to reliable observations, a key requirement concerns the number of the observed events, which has to be statistically relevant (for the e^+ fluence available, up to 50 million events are collected per each implantation energy).

In Fig. 2.12 are also indicated the line shape parameters S and W, also referred to as low and high momentum parameters. They are defined as the ratio between the events detected in the central window and in the wings of the annihilation peak (indicated as A_S and A_W in Fig. 2.12), with respect to the total number of events. Considering the case of a material containing vacancy defects (missing atoms in the lattice that creates nano-voids) needed to accomodate positrons, subsequent annihilation with electrons will provide information about the atoms surrounding this cavity. If the momentum of thermalized positrons is negligible as compared to the one of electrons on a defect, the S parameter measured in the PAS-Db mode will contain information about the *valence* electrons of these atoms. At the same time, the W paramenter, being by definition a high-momentum parameter, will contain information about the *core* electrons. Despite this general consideration, these parameters are mostly meaningless by themselfes, but still allow for correlative analysis of

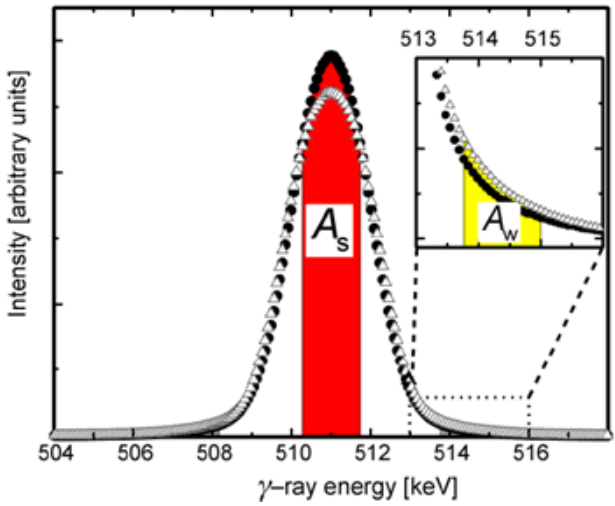


Figure 2.12: Representation of a recorded Doppler spectrum: number of annihilation events per received γ-photon energy. The two windows used for the calculation of the S and W parameters are also indicated.

different experiments leading to a meaningful insight.

For example, in a multi-layered structure, such as an MOS device, the analysis of the S- and W- parameters as a function of the implantation energy represents a powerfull tool to probe the interface characteristics. In this case, the measured S- and W- parameters will reflect superposition of different broadening components, each one associated with a characteristic positron annihilation state inside the sample. In presence of only two positron annihilation states (e.g., at the surface and in the bulk), the measured S and W parameters can be expressed as linear combinations of the surface and bulk contributions:

$$\begin{aligned} S_{\text{measured}} &= A_{\text{S}} S_{\text{surface}} + B_{\text{S}} S_{\text{bulk}} \quad , \\ W_{\text{measured}} &= A_{\text{W}} W_{\text{surface}} + B_{\text{W}} W_{\text{bulk}} \quad . \end{aligned} \tag{2.21}$$

With increasing positron acceleration energy and, therefore, the positron implantation depth, one will find the S, W values to evolve along a straight line connecting the two characteristic states on the (S, W) plane. Would non-linear behavior be observed in this (S, W) plot, it will then point towards the presence of additional annihilation states.

At the same time, clustering of points in the (S, W) plot would

suggest that, despite the increasing implantation energy, positrons annihilate in approximately the same environment, thus producing approximately the same S and W values.

The analysis of the S- and W-parameters as a function of the implantation energy can also provide valuable information. However, as mentioned above, positrons are not implanted at a single depth but for each energy a broad implantation profile is generated depending on the sample structure and characteristics. This not only prevents the analysis of thin films (< 100 nm), but also implies that, in the analysis of the recorded S- and W- parameters at each implantation energy, one has to take into account simultaneous events occurring at different depths. Importantly, this effect increases with the e^+ implantation depth (positrons implanted deeper in the sample will have a wider implantation profile). To a certain extent, this problem can be addressed by using commercially available software tools for the estimate of such implantation profiles (i.e., VepFit, RoyProof).

PAS in the Db mode is a powerful tool for defect analysis, but might suffer from poor selectivity since the observation of photons with a specific energy provides no information regarding the source of the received photons. A way to increase the selectivity is to perform PAS experiments in 1D coincidence DB mode. In this configuration, the instrument is provided with a second γ-ray detector positioned at 180° from the first detector. In this way, one can choose to collect only the photons that are received *simultaneously* by the two detectors, thus ensuring that they originate from an annihilation event within the studied sample. This adjusted technique has the advantage of strongly reducing the measurement noise, especially in the high-momenta window of the measured spectra. However, the coincidence condition also critically limits the number of events count and, consequently, increases the measurement time up to one order of magnitude.

In the coming experimental sections, applications of the described electrical and physical characterization techniques in a correlative manner will be demonstrated. We will address the whole spectrum of defects encountered in the (Si)Ge/insulator structures ranging from the interface dangling bonds to oxide defects.

Bibliography

[1] E.H. Nicollian and J.R. Brews *MOS(Metal Oxide Semiconductor) Physics and Technology* (Wiley-Interscience, NewYork, 1982)

[2] R. Engel-Herbert, Y. Hwang, and S. Stemmer *Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces*

J. Appl. Phys., **108**, 124101 (2010)

[3] C.N. Berglund *Surface states at steam-grown silicon-silicon dioxide interfaces* IEEE Trans. Electron Dev., **13**(10), 701 (1966)

[4] P.V. Gray, and D.M. Brown *Density of SiO_2/Si interface states* Appl. Phys. Lett., **8**, 31 (1966)

[5] D.M. Brown, and P.V. Gray *Si-SiO_2 fast interface state measurements* J. Electrochem. Soc., **115**, 760 (1968)

[6] N.H. Thoan, K. Keunen, V.V. Afanas'ev, and A. Stesmans *Interface state energy distribution and P_b defects at (110)Si/SiO_2 interfaces: Comparison to (111) and (100) silicon orientations* J. Appl. Phys., **109**, 013710 (2011)

[7] N.H. Thoan, M. Jivanescu, B.J. O'Sullivan, L. Pantisano, I. Gordon, V. Afanas'ev, and A. Stesmans, *Correlation between interface traps and paramagnetic defects in c-Si/a-Si:H heterojunctions* Appl. Phys. Lett., **100**(14), 2101 (2012)

[8] Y. Lam *Interface studies of the m.i.s. structure by surface photovoltage measurements* Electronics Lett., **6**(6), 153 (1970)

[9] Y. Lam *Surface-state density and surface potential in MIS capacitors by surface photovoltage measurements. Part I* J. Phys. D: Appl. Phys., **4**, 1370 (1971)

[10] L. Kronik, and Y. Shapira *Surface photovoltage phenomena: theory, experiment, and applications* Surf. Sci. Rep., **37**, 1 (1999)

[11] H. Yamagishi *Fermi level stabilization and surface states at interfaces of Si(111) surfaces and insulating layers* J. Phys. Soc. Jap., **25**(3), 766 (1968)

[12] L. Terman *An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes* Solid State Electr., **5**, 285 (1962)

[13] J.R. Hauser, CVC software, http://ece.ncsu.edu/research/tool

[14] O. Johnson *Large signal surface photovoltage studies with germanium* Phys. Rev. B, **111**(1), 153 (1958)

[15] V. Afanas'ev, and A. Stesmans, *Photoionization of silicon particles in SiO_2* Phys. Rev. B, **59**(3), 2025 (1999)

[16] V. Afanas'ev, and A. Stesmans, *Stable trapping of electrons and holes in deposited insulating oxides: Al_2O_3, ZrO_2, and HfO_2* J. Appl. Phys., **95**(5), 2518 (2004)

[17] W.C. Wang, PhD dissertation: *Internal Photoemission, Photoconductivity, and Photodepopulation in Ultrathin Layers of Oxide Insulators for Memory Applications*, KULeuven, May 2014

[18] V.V. Afanas'ev, W.C. Wang, F. Cerbu, O. Madia, M. Houssa, and A. Stesmans, *Spectroscopy of Deep Gap States in High-k Insulators* ECS Trans., **64**(8), 17 (2014)

[19] J. Kepa, PhD dissertation: *Electron spin resonance study of degradation of SiGe/SiO_2 structures and of c-Si foils and CuInSe absorber layers for photovoltaic application*, KULeuven, Sept 2015

[20] P.J. Caplan, E.H. Poindexter, B.E. Deal, and R.R. Razouk *ESR centers, interface states, and oxide fixed charge in thermally oxidized silicon wafers* J. Appl. Phys., **50**, 5847 (1979)

[21] E.H. Poindexter and P.J. Caplan *Characterization of Si/SiO_2 interface defects by electron spin resonance* Progr. Surf. Science, **40**, 201 (1983)

[22] J.E. Wertz and J.R. Bolton, *Electron Spin Resonance: Elementary theory and practical applications* 2^{nd} *ed.* (McGraw-Hill Book Company, New York, 1986)

[23] F. Tuomisto, and I. Makkonen *Defect identification in semiconductors with positron annihilation: Experiment and Theory* Rev. Mod. Phys., **85**(4), 1583 (2013)

Chapter 3

Ge P_{b1} centers at interfaces of condensation-grown SiGe layers with SiO_2

The success of a technology employing a high-mobility Ge-based channel in MOS devices crucially depends on the availability of a fabrication technique that combines low costs and high electrical quality of the channel/insulating stack interface, where the latter implies a low interface defect density.

Among the possible routes to the Ge MOS technology, the **Ge condensation** technique [1][2] -a growth method- offers a number of advantages since it enables the growth of high-Ge content SiGe layers over large wafer areas. Moreover, this fabrication process delivers $Si/SiO_2/Si_{1-X}Ge_X/SiO_2$ heterostructures that naturally isolate the SiGe channel from the Si substrate and hence benefit from the possibility of implementation of semiconductor-*on-insulator* device structures (more details will be discussed in Section 3.3). The goal of this chapter is to investigate the defects at interfaces of $Si_{1-X}Ge_X$ layers in these stacks, aiming at the evaluation of the feasibility (practical implementation) of the Ge-condensation technology.

Intuitively, one might expect that the $SiGe/SiO_2$ interface would closely resemble the standard Si/SiO_2 interface. Thus, at the beginning of this chapter, a brief description of the main defect controlling the electrical quality of the Si/SiO_2 interface in MOS devices, namely the **Si dangling bond** (DB), is provided.

Surprisingly enough, the search for a similar **Ge DB** defect has been unsuccessful for long time and only in 2009, ESR performed on the condensation-

grown $SiO_2/Si_{1-X}Ge_X/SiO_2$ heterostructures provided proof of the Ge DB existence, as will be briefly overviewed in the second section of this chapter.

Next, novel experimental results will be presented that address the physical factors determining the generation of the interfacial Ge DBs, as well as the efficiency with which they can be inactivated (passivated) by hydrogen. These observations will be correlated with the presence of **residual strain** in the $Si_{1-X}Ge_X$ layers fabricated using the condensation technique.

In the last section, the charge state of the Ge DB centers will be further investigated through a series of PAS experiments (Chapter 2 Section 5) .

3.1 The Si dangling bond defect

As already mentioned in the introduction, while in the early days of the Si-based microelectronics major degrading factors were related to the presence of impurities or contaminants in the semiconductor and the insulating layers [3], significant improvements in purity of materials and processing have shifted the attention towards intrinsic defects.

Despite SiO_2 providing an high quality insulator on Si, the lattice (network) mismatch between the two different materials and a certain amount of thermal shear stress, were concluded to concur in the creation of defects during the formation of the SiO_2 layer [4]. Specifically, *broken (dangling) bonds at the interface between the Si and the SiO_2 layers were found to be electrically active and thus detrimental for device operations.*

Different "flavors" of such DB defects can be spectroscopically isolated, depending on the orientation of the host Si crystal. As an example, Fig. 3.1 shows atomic models of **Si DBs** found at the interface between a (100) oriented Si surface and SiO_2. For this surface orientation, ESR specroscopy resolves two types of DBs defects labelled P_{b0} and P_{b1}, respectively. Interestingly, the P_{b0} center on (100) Si is very similar the P_b center, the only major DB defect observed at the oxidized Si (111) face. As illustrated in Fig. 3.1, the P_{b0} center resides on a (111) facet of the (100)-orientated Si crystal face. By contrast, the P_{b1} center is structurally different, as it pertains to a DB adjacent to a strained Si-Si dimer.

In the neutral state, each broken bond contains an unpaired electron (indicated in Fig. 3.1 as a single short arrow), which makes it paramagnetic (ESR active). Furthermore, P_b and P_{b0} give rise to two distinct energy levels within the forbidden gap of Si (Fig. 2.2). As a result, depending on their energy position with respect to the Fermi energy at the semiconductor surface, they can adquire or release an electron, thus making the DB defect operating as an interface trap [5] [6] [7].

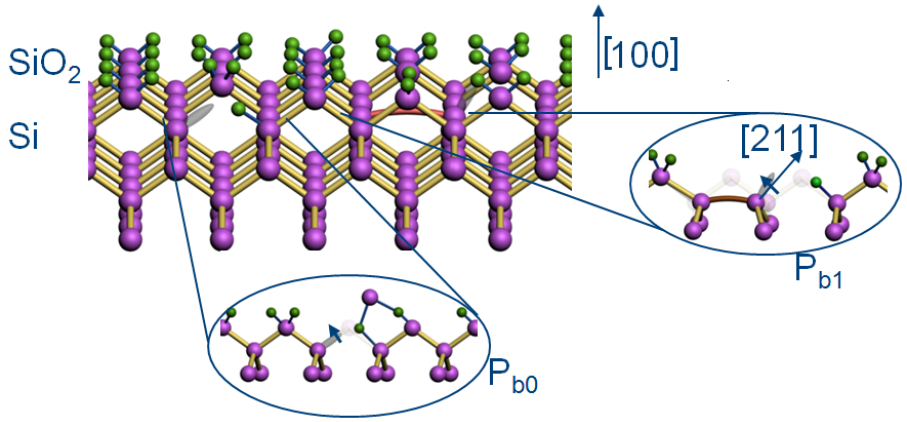


Figure 3.1: Ball-and-stick model for the (100)Si/SiO_2 interface. The two main type of dangling bond defect are shown: The Si P_{b0} and the Si P_{b1} centers.

For the specific case of Si MOS devices, it is well known that defects associated with Si DBs constitute the **dominant** contribution to the observed density of interface traps. An overview of the corresponding $D_{IT}(E)$ distributions, as resolved by CV and AC conductance methods, on the three main Si surface orientations, is presented in Fig. 3.2 [8]. Here, "0" on the energy axis corresponds to the VBT of silicon. It is clearly seen that different defect densities are generated upon oxidation of Si substrates of different orientation. However, two $D_{IT}(E)$ peaks at about 0.2 and 0.85 eV above the VBT emerge as a common feature. This recognizable feature of Si DBs is found to correspond to the energy level at which these defects trap or release an electron (0/- and 0/+ charge transition levels).

In Fig. 3.2 are also shown the densities of active defects left after *passivation treatment, i.e. annealing in H_2*, when the DBs are saturated by bonding to a H atom[1]. This passivation is seen to be so effective that forming gas anneal is nowadays repeated multiple times during device fabrication. Nonetheless, some of those Si:H bonds can still break during device operation (*de-passivation*), causing degradation of the device performance over time.

The kinetics of the interaction between the dangling bond of Si and hydrogen was found to be consistently and accurately described by the so-called Generalized Simple Thermal model, or GST [9][10], which accounts for a

[1]The possibility of reducing the density of such electrically active defects to a level below $5\times\ 10^{11}$ cm^{-2} is what ultimately set forth the unrivaled success of Si over other channel materials.

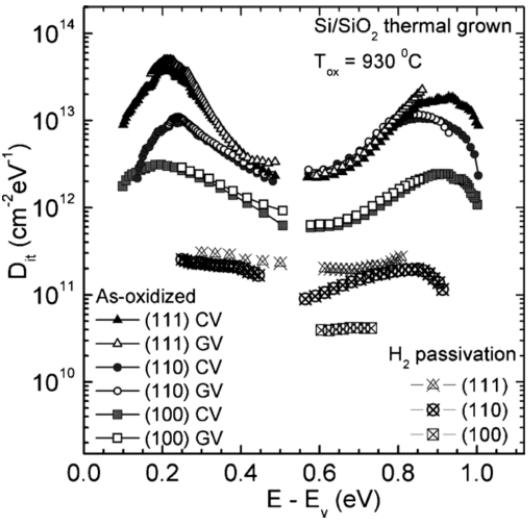


Figure 3.2: Density of interface traps energy distribution ($D_{IT}(E)$) as estimated by the high-low frequency CV method (solid symbols) and by the AC-conductance method (indicated as GV, open symbols) on (100), (110) and (111) Si/SiO_2 samples. Also reported are results as estimated on samples subjected to defect passivation anneal in molecular hydrogen (30 min, 1.1 atm, T = 400 $°C$). Image from Ref. [8].

simultaeous occurrence of both formation and dissociation of the Si:H bonds.

Importantly, it was demonstrated that the presence of the Si DB defects has a “universal" character, as the same P_bs ESR signals were also reported at interfaces between Si and high-k oxides such as HfO_2, ZrO_2 and Al_2O_3 [11][12][13], as well as Si and Si_3N_4 and GaN. As mentioned before [12], on first notice this would indicate the Si/oxide interface, within its first arom layers, to be of a Si/SiO_2 nature. The omnipresence of the Si DBs at different interfaces suggest these defects to be the archetypal mismatch-induced imperfections. Therefore, it would be logical to expect the presence of the DB-type defects at interfaces of other semiconductors with oxide or nitride insulators.

3.2 The Ge dangling bond

Following the above considerations, the search for interfacial paramagnetic Ge DB centers has been conducted for a while, however, with only limited success.

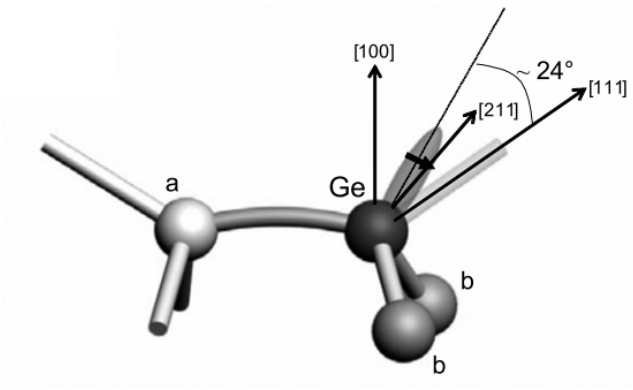


Figure 3.3: A ball-and-stick schematic representation of the Ge P_{b1} center. The letters "a" and "b" may represent different atoms of Si or Ge. Image from Ref. [20]

No measurable contribution of the Ge DB defects to the interface trap density was found at interfaces of Ge with GeO_X, HfO_2 and Al_2O_3 [14] [15]. In an attempt to explain these observations, some researchers advanced the hypothesis that DBs of Ge do not provide energy levels in the semiconductor band gap [16], making them not detectable by ESR.

Only in 2008 the presence of DB defects in oxidized germanium was demonstrated by electrically-detected spin resonance [17]. However, no estimate of their density was provided thus impeding correlation with electrical data.

Meanwhile, several authors have succesfully traced (interfacial) Ge DBs in SiGe alloys in the past. A first observation of a defect assigned to Ge was reported as early as 1992 [18] on O-implanted $Si_{0.9}Ge_{0.1}$ and $Si_{0.6}Ge_{0.4}$ crystals. Similar observations came also from other groups [19]. Finally, in 2009, successful detection of a substantial density of Ge DB-type centers was reported at interfaces of $Si_{1-x}Ge_x$ with SiO_2 for a wide range of Ge concentrations ($0.28 < x < 0.93$) [20][21].

Fig. 3.3 schematically shows the proposed atomic structure of this defect: A DB of a Ge atom pertaining to a strained Ge-Si dimer (in Fig. 3.3 the letters "a" and "b" may represent Si or Ge atoms, and serve to indicate the most likely composition ratio for this defect). Considering the similarity to the earlier described Si DB centers (see, e.g., Fig. 3.1) this defect was labeled Ge P_{b1} center.

Using the same samples, it appears possible to correlate ESR results and electrical data revealing that Ge P_{b1} centers in $Si_{1-x}Ge_x$ behave as

shallow acceptors [22]. A nearly one-to-one correlation between the densties of paramagnetic defects, as estimated by ESR experiments, and the densities of negative fixed charges was since reported several times since then [22][23]. These evidences suggest a fundamental difference in electrical properties of this defect as compared to the amphoteric defects encountered at the Si/SiO_2 interface.

At the same time, the ability of Ge DBs to react with molecular hydrogen appear similar to the behavior of Si DBs [24]: A study performed on samples with a $Si_{0.27}Ge_{0.73}$ layer indicated that Ge P_{b1} centers can be partially passivated by annealing at 500 $^{\circ}C$ for 1 h in H_2 (1 atm) [22]. However, this passivation process appears to be not as efficient as on Si/SiO_2 samples [24] leaving the density of active defect in the $10^{11} - 10^{12} cm^{-2}$ range (as can be seen in Fig. 3.2, the same passivation anneal on Si/SiO_2 samples produces much lower defect densities).

A more detailed passivation study [24][25] reveals that the kinetics of the reaction between the Ge DB and H_2 is still described by the GST model, but accounting for the existence of a significant spread in the activation energies of the two reactions (passivation and dissociation). The overlap of the two distributions in activation energies resulting from this spread implies that the $Si_{1-x}Ge_x/SiO_2$ interface cannot be passivated to the same degree as the Si/SiO_2 interface.

3.3 The Ge-condensation growth method

Description of the samples

The semiconductor-on-insulator concept is particularly attractive in developing (Si)Ge channel layers which, as discussed in the introduction, needed to be integrated on a Si carrier wafer. If successful, these Germanium-On-Insulator (GOI) substrates would combine the benefits of Ge high-mobility with the advantages of the semiconductor-on-insulator architecture. It is in this context that the **Ge condensation growth** has been developed [1].

This two-step process is schematically represented in Fig. 3.4. To start, a 200 mm diameter SOI wafer with 22 nm thick boron doped ($5 \times 10^{17} atoms/cm^3$) top Si layer and a 140 nm thick buried oxide (BOX) layer is used. Next, a Si-rich $Si_{1-y}Ge_y$ (y = 0.24 - 0.27) layer is epitaxially grown, using SiH_4 and GeH_4 as precursors in an ASM Epsilon©2000 reactor. As it is shown in Fig. 3.4, the stack is completed by a thin (7 nm) epi-Si layer aiming to prevent out diffusion of Ge during the early stage of the thermal oxidation process.

Next, selective oxidation of Si atoms is carried out by exposing the sample to temperatures above the range of thermal stability of Ge oxides. Two

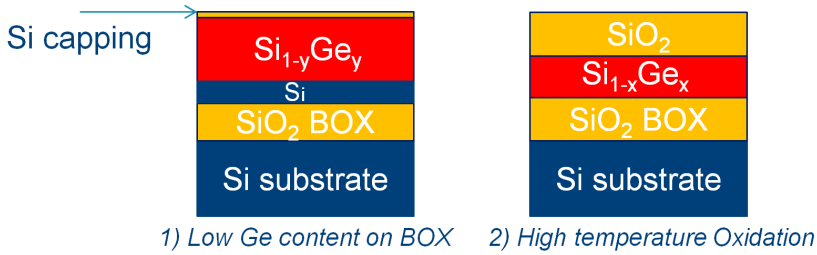


Figure 3.4: Illustration of the two-step fabrication process of the SiGe-On-Insulator layers.

concomitant phenomena take place: First, oxidation of Si into SiO_2 at the top interface (SiO_2 represents the only oxide stable at this temperature). Second, diffusion of Ge atoms through the SiGe and the Si layers of the SOI. As a result, piling-up of Ge at the oxidizing top interface is prevented, thus leading to a gradual Ge enrichment of the entire $Si_{1-y}Ge_y$ layer. This process is represented as the second step in Fig. 3.4. In order to keep the oxidation temperature below the (Si)Ge melting point, three steps of dry oxidation (at 1150, 1000 and 900 $°C$), each followed by annealing in inert (Ar) ambient have been performed.

The samples used in this work were also subject to the deposition of Al blankets on the backside and sidewalls of the samples to ensure reliable contact with the $Si_{1-x}Ge_x$ layer sandwiched between two SiO_2 insulators. Finally, MOS capacitors were fabricated by evaporating Al electrodes through a shadow mask on the top oxide (TOX) layer.

Two sets of samples were prepared by using initial $Si_{1-y}Ge_y$ layers of different initial thickness and different oxidation time. The composition and the thickness of the resulting $Si_{1-x}Ge_x$ layers are listed in Table 3.1.

3.4 Impact of strain on generation and passivation of Ge P_{b1} centers

As already mentioned in the previous sections, unlike the amphoteric Si DBs, the Ge P_{b1} center appears to behave electrically as a shallow acceptor. This was established by observing the temperature-dependent shift of CV curves measured at room temperature and at 77K: The Fermi level in a semiconductor will change its position with the temperature of the sample, causing a Grey-Brown shift of the CV characteristic (Chapter 2 Section 1.3). An example of such shift, as measured on the $Si/SiO_2/Si_{0.45}Ge_{0.55}/SiO_2/Au$ heterostructure is

Table 3.1: Composition and thickness of the $Si_{1-x}Ge_x$ layers. The two sets describe the samples fabricated starting from initial $Si_{1-y}Ge_y$ layers of different thicknesses. The final Ge concentration was determined by means of Rutherford BackScattering (RBS) analysis.

104nm $Ge_{0.27}Si_{0.73}$			
No.	Ge fraction	Ge_xSi_{1-x} layer thickness (nm)	TOX thickness (nm)
1	0.45	54	150
2	0.58	57	170
3	0.70	46	195
4	0.73	45	195
5	0.93	27	210
64nm $Ge_{0.24}Si_{0.76}$			
No.	Ge fraction	Ge_xSi_{1-x} layer thickness	TOX thickness
6	0.28	64	84
7	0.42	34	120
8	0.55	27	135
9	0.65	24	148
10	0.75	16	155
11	0.87	15	158

shown in Fig. 3.5, together with 100 kHz CV curve as measured at T = 77K on the sample containing 70 % of Ge in the SiGe layer.

The observed decrease of the capacitace at sufficiently large positive gate bias indicates depletion of the SiGe films suggesting the p-type conductivity of the $Si_{1-x}Ge_x$ layers. Then, the temperature-induced shift of the CV curves towards more negative voltages indicates that a lower electric field is required to deplete the semiconductor as temperature becomes lower. From these observations one can conclude that, when the Fermi level is shifted closer to the Valence band maximum at low temperature, negative charges are released, which corresponds to acceptor-like behavior of defects.

The threshold voltage V_T of the CV curves may also be used to obtain information regarding the density of negative charges. As briefly explained in the previous chapter, in an ideal case, a p-type MOS structure would start to deplete from majority carriers when the gate potential becomes positive. Assuming zero work function difference between the Au gate and the p-type $Si_{1-x}Ge_x$ layer, one can estimate that the areal density of negative charges from the specific V_T needed to deplete the semiconductor is:

$$Q = V_T \times C_{TOX} \tag{3.1}$$

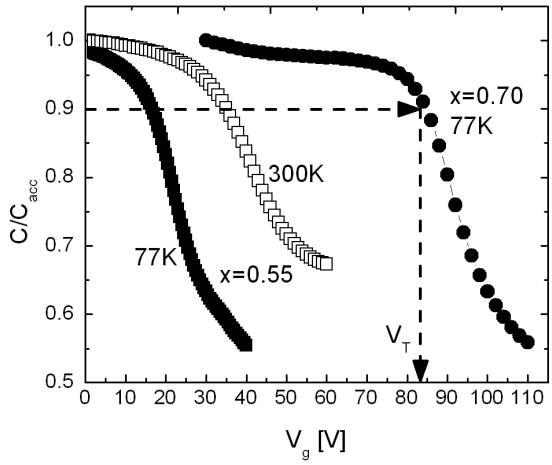


Figure 3.5: 100 kHz CV curves measured, at room temperature and at 77 K (open and solid symbols, respectively), on samples containing 55 % and 70 % of Ge in the $Si_{1-x}Ge_x$ layer. An estimated threshold voltage V_T, corresponding to the onset of depletion of the $Si_{1-x}Ge_x$ layer, is defined as the voltage at which the measured capacitance drops of 10 %.

where C_{TOX} represents the capacitance value of the top oxide layer. As indicated in Fig. 3.5, we define V_T as the gate voltage at which the measured capacitance has dropped by 10 %. In the rest of this section, the areal density of negative charges as a function of Ge fraction is monitored both in the as-received samples and after different passivation anneals (30 $\pm$ 1min in 1 atm H_2), using the 100 kHz CV traces at 77K.

As reported by Souriau et al. [2], the lattice constant of the $Si_{1-x}Ge_x$ alloy increases with the Ge content. At the same time, oxidation of Si into SiO_2 increases the molar volume of the material. As a consequence, during the condensation process the $Si_{1-x}Ge_x$ layer experiences high levels of stress that leads to generation of extended and point defects to partially accommodate the mismatch of the SiGe film with the TOX and BOX layers.

The residual strain values in the $Si_{1-x}Ge_x$ layer estimated using the high-resolution X-ray diffraction (HR-XRD) technique are plotted in Fig. 3.6(a) as a function of Ge concentration. It can be seen how, starting from the low Ge concentration ($x \leq 0.27$) the residual strain in the $Si_{1-x}Ge_x$ film initially increases with x and reaches a maximum at around $x \approx 0.7$. For higher Ge concentrations, generation of dislocations in the $Si_{1-x}Ge_x$ layer occurs leading to partial relaxation of the strain [26].

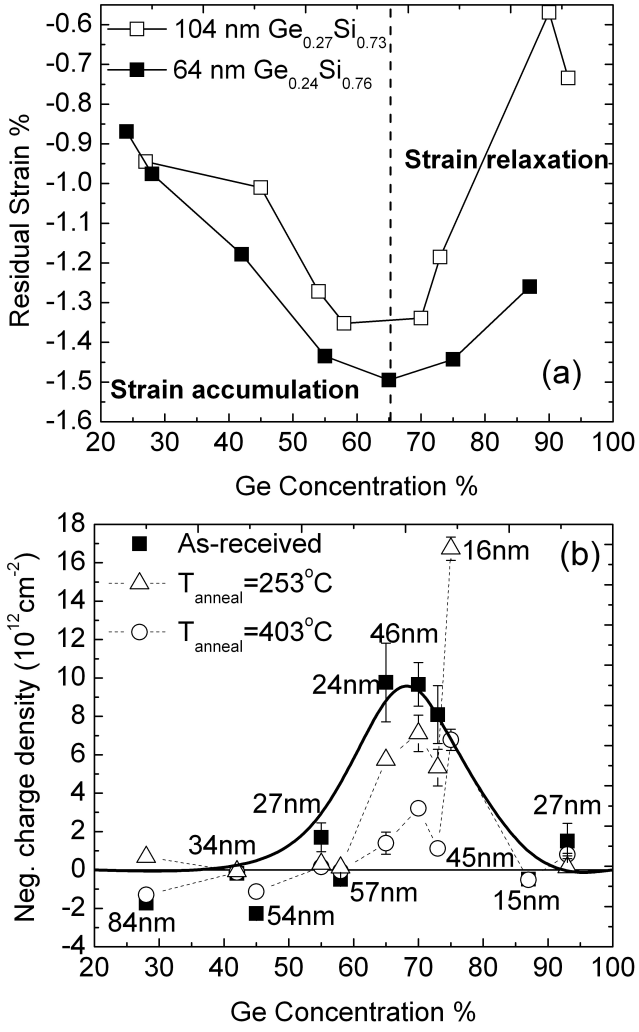


Figure 3.6: (a) Residual strain in the $Si_{1-x}Ge_x$ layer as a function of Ge content, as measured by HR-XRD. Results are presented separately for the two sets of samples fabricated by the Ge condensation starting from different thicknesses of the initial GeSi films (104 nm and 64 nm). The final concentration of Ge was determined by RBS. (b) Density of negatively charged defects as a function of Ge concentration, as determined from the threshold voltage on CV curves measured atT = 77 K on the as-received samples (solid squares) and in samples passivated by annealing in H_2 for 30 min at 253 $°C$ or 403 $°C$ (open triagles and open circles, respectively). The thicknesses of the semiconductor layers are indicated on each result. The bold solid curve guides the eye.

Also worth mentioning is a substanctial dependence of the residual strain on the thickness of the $Si_{1-x}Ge_x$ layer. The second set of samples (filled squares in Fig. 3.6(a)), fabricated starting from a thinner initial $Si_{1-x}Ge_x$ layer than the first set of samples, shows a generally increased residual strain by $\approx 0.2\%$. Apparently, the thinner $Si_{1-x}Ge_x$ layers are less prone to formation of misfit dislocations which makes this mechanism of strain relief less effective than in thicker semiconductor layers.

As can be seen from the defect densities shown in Fig. 3.6(b), at the chosen anneal temperatures of 253 $^\circ C$ and 403 $^\circ C$ we were be able to passivate between 50 % and 93 % (depending on x) of the defects in the first set of samples used in this work (numbers 1 to 5 in Table 3.1) [20] [22]. The CV measurements performed on the x = 0.75 sample (sample #10 in Table 3.1) in the as-received state did not allow us to reach depletion in the GeSi layer because of TOX dielectric breakdown. Nevertheless, one can refer to the observed breakdown voltage to estimate the lower limit of density of negative interfacial charges in this sample to be $1.7 \times 10^{13} cm^{-2}$.

Several results suggest the influence of the residual strain on the formation of the observed defects. First, starting from a minimum defect density in the Si-rich samples, the maximum density is reached when the $Si_{1-x}Ge_x$ layer is strained to the maximum [in the range $(0.6 < x < 0.8)$]. Both the strain and the charge density are seen to decrease for higher Ge concentrations, suggesting the possibility that both phenomena are governed by a common physical mechanism. Second, the data show that the generation of negative charges is enhanced by a relatively small increment of the residual strain in the $Si_{1-x}Ge_x$ layer.

A representative case is provided by the samples listed in Table 3.1 as numbers #4 and #10. While both of them have nearly the same Ge content (x = 0.73 and 0.75, respectively), the thickness of the $Si_{1-x}Ge_x$ layer in the second sample is smaller by a factor of ≈ 3 (16 nm versus 45 nm). This transition to a thinner $Si_{1-x}Ge_x$ layer reveals an increase of negative charge density from $8.1 \times 10^{12} cm^{-2}$ in 45-nm $Si_{1-x}Ge_x$, to more than $1.7 \times 10^{13} cm^{-2}$ in the 16-nm $Si_{1-x}Ge_x$. Taking into account nearly the same Ge concentration, the increase of the defect density can be correlated with the increase of the residual strain indicated by the XRD data and shown in Fig. 3.6(a).

The analysis of defect densities in the samples with different degree of hydrogen passivation [open triangles and circles in Fig. 3.6(b)] suggests that the enhanced strain may also severely reduce the efficiency of the passivation. By comparing the densities of negative charges found in the two sets of samples with different thickness of the $Si_{1-x}Ge_x$ layer after passivation by annealing in hydrogen for 30 min at 403 $^\circ C$ (Fig. 3.7), we can see that the fraction of defects resistant to the passivation is enhanced in the samples with a thinner $Si_{1-x}Ge_x$ film. For example, for samples #4 and #10 discussed above, the density of unpassivated defects differs by a factor of ≈ 7, as indicated by the bold arrow

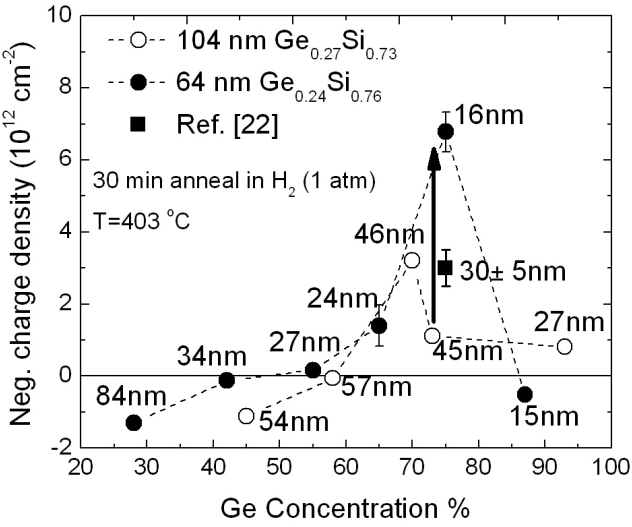


Figure 3.7: Negatively charged defect density as a function of Ge concentration, as evaluated after passivation anneal in H_2 for 30 min at 403 $°C$. Results are presented separately for the two set of samples fabricated starting from different thicknesses of the initial SiGe films (104 nm and 64 nm as indicated). Data from Ref. [25] are also included for comparison. The bold arrow indicates the effect of an increased residual strain on the density of defects resistant to the passivation process.

in Fig. 3.7.

Thus, a number of elements support the hypothesis that residual strain in the Ge_xSi_{1-x} critically affects both the initial density of Ge dangling bonds, and the efficiency of their passivation by molecular hydrogen.

3.5 Charge transition level of Ge P_{b1} centers

As mentioned in Section 3.2, the density of paramagnetic Ge P_{b1} centers estimated by using ESR spectroscopy as a function of Ge content, and shown in Fig. 3.8, matches **quantitatively** the density of the negative charges observed using CV measurements (Fig. 3.6(b)) [22].

This correspondence raises a question related to the fact that ESR experiments, performed at 4.2K, are limited to probing the defects in the paramagnetic state, such as single occupied DB defects. However, formation

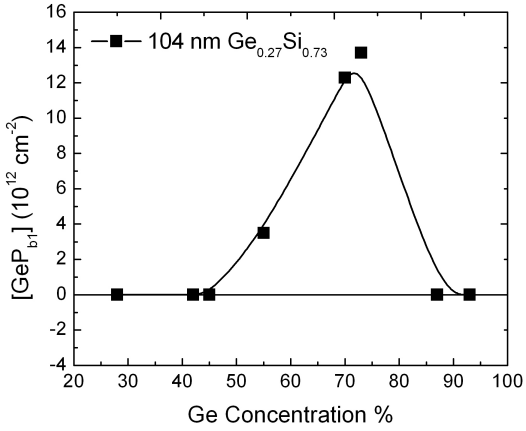


Figure 3.8: Areal density of [GeP_{b1}] paramagnetic centers as probed by ESR spectrometry on the $Si_{1-x}Ge_x/SiO_2$ heterostructures as fabricated starting from an initial 104 nm thick $Si_{0.73}Ge_{0.27}$ layer (first set of samples in Table 3.1). Additional data points have been added from Ref. [20]. The bold solid curve guides the eye.

of a negatively charged center detected by CV measurements at 77K or 300K would require capture of an additional electron which would turn the defect in ESR-inactive state.

The possible explanation of this consists in the variation of the relative position of the defect (0/-) charge transition level with respect to the Fermi energy in the sample at the different temperatures: When the charge state of such defects is assessed at 77K, most of the Ge P_{b1} centers doubly occupied are negatively charged, suggesting that their energy level is still below the Fermi level in $Si_{1-x}Ge_x$. However, when the samples are cooled down to 4.2K for the ESR experiments, the SiGe Fermi level moves toward the VB edge, crosses the (0/-) transition level and, as a consequence, most of the defects become neutral. This hypothesis is illustrated in Fig. 3.9.

To verify this hypothesis we appealed to PAS spectroscopy, because this experimental method is capable of monitoring the behavior of the negatively charged defects over the whole temperature range from room temperature to 4.2K.

Fig. 3.10(a) shows the PAS S-W plots obtained from room temperature experiments performed on sample #10 ($Si_{0.25}Ge_{0.75}$ layer) prior- and after defect

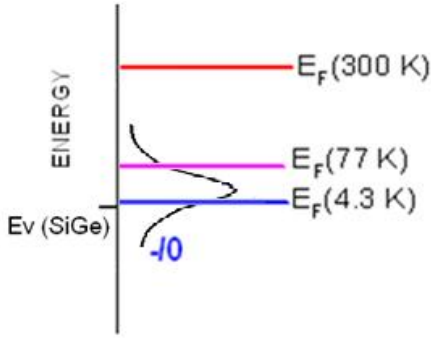


Figure 3.9: Schematic illustration of the position of the Fermi level in the $Si_{0.27}Ge_{0.73}$ layer band gap as a function of the sample temperature, together with the proposed charge transition level of the Ge P_{b1} centers

passivation in molecular hydrogen. The solid curves indicate the evolution of the S-W pairs with increasing positron implantation energy.

As mentioned in Chapter 2, the S-W plot is able to reveal the presence of different positron trapping states. As can be seen in Fig. 3.10(a) at low implantation energies, a clustering of points in the as-received sample (filled squares), indicates the presence of a specific positron trapping site [27][28]. This state, however, disappears after the DB passivation in H_2 (open squares in Fig. 3.10(a)) indicating that the detected state is related to the Ge DB defects.

In Fig. 3.10(b) the similarly obtained S-W plot is shown for the sample with x = 0.73 (#4 in Table 3.1). Also in this sample the (S, W) pairs measured at low implantation energies concentrate in the same region of the (S, W) plane. However, the resulting cluster is spread over a larger plot area. Due to the lower density of negative charges, a lower sensitivity of the PAS technique to this particular positron trapping site may be expected. Nevertheless, as in sample #10, a similar change in the S-W trend, i.e. disappearance of the DB-related ''cluster" of S-W values, is found after passivation (open squares in Fig. 3.10(b)). The similarity of these results indicates that the positron trapping state present in sample #10 is also present in sample #4.

Finally, Fig. 3.10(c) and (d) shows the S-W plots as obtained from samples #7 and #11, containing 42 % and 87 % Ge in the $Si_{1-x}Ge_x$ layer. These results do not exhibit any specific trend, which is consistent with low density of negatively charged Ge DB centers [c.f. Fig. 3.6(b)].

To futher support the inferred association of the positron trapping sites to Ge DB defects, Fig. 3.11 shows the value of the S-parameter, as measured on samples #4 and #10 before and after defects passivation anneal, as a function

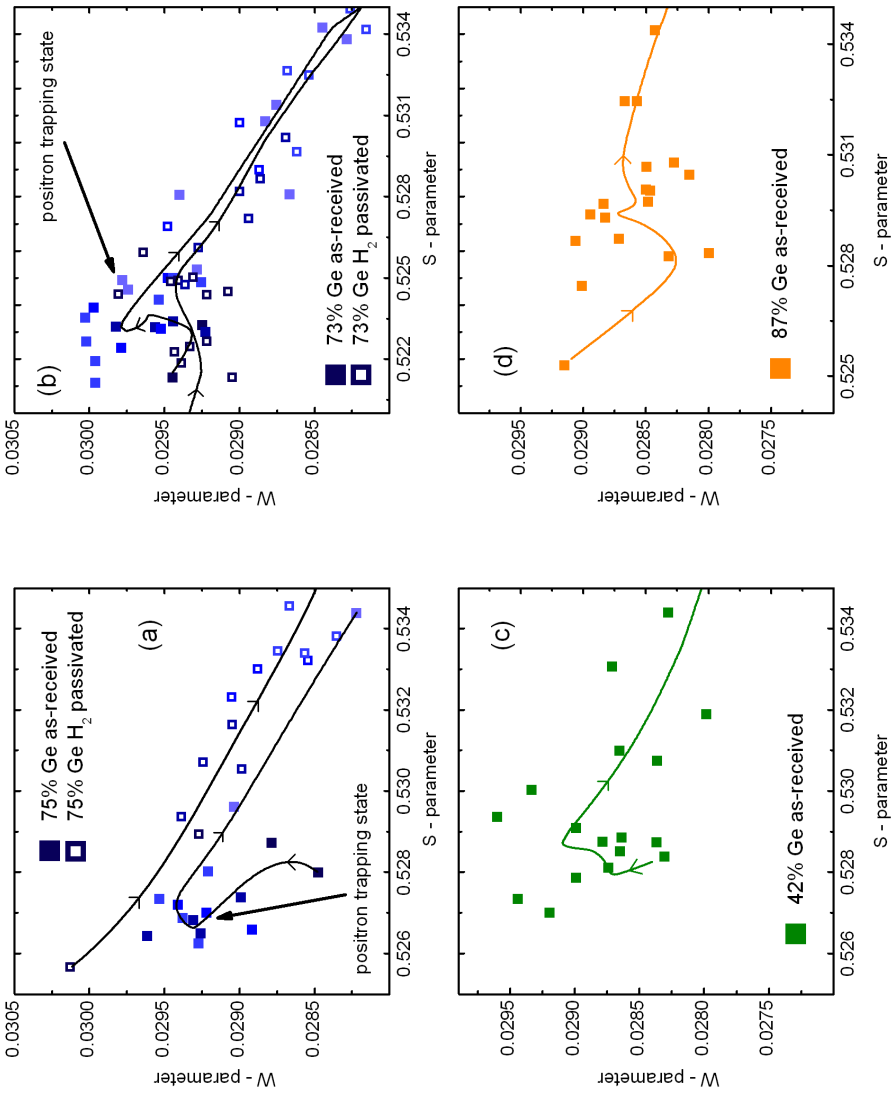


Figure 3.10: The line shape parameters (S, W) measured in the (100)$Si/SiO_2/Si_{1-x}Ge_x/SiO_2$ samples containing 75% (a), 73% (b), 42% (c) and 87% (d) Ge in the $Si_{1-x}Ge_x$ layer. PAS Db mode measurements on samples containing 75% and 73% Ge, panels (a) and (b), have been performed prior- and after defects passivation by H_2 (filled and hollow symbols, respectively). The solid curves indicates S-W evolution with increasing positron acceleration energies.

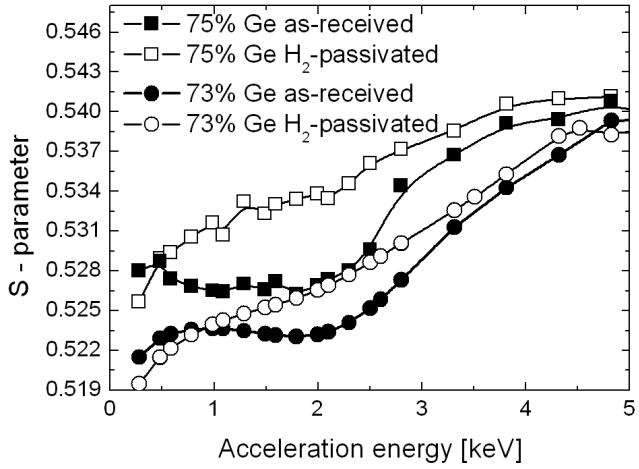


Figure 3.11: S-parameter as a function of positron implantation energy, as measured in samples #10 and #4, containing 75 % and 73 % of Ge in the Ge_xSi_{1-x} layer (indicated by squared and circles symbols, respectively) prior- and after passivation anneal in molecular hydrogen (solid versus open symbols).

of the positron implantation energy (related to the mean implantation depth). At positrons acceleration energies close to 2 keV, we are able to implant e^+ at a mean depth of $\approx$ 180 nm, i.e., close to the top $SiO_2/Si_{1-x}Ge_x$ interface.

For e^+ implantation energies $\leq$ 2.5 keV a plateau of the S-parameter can be observed in both samples in the as-received (un-passivated) state. This suggests the presence of a trapping site that reduces the diffusion length of positrons: Despite the increasing implantation energy, positrons annihilate approximately in the same enviroment and, as a result, the same S-parameter value is measured.

Upon passivation of the defects by hydrogen and elimination of negative charges, the S-parameter variation on the positron implantation energy is clearly changed: In this same range of energies a monotonic increase of the S-values with increasing acceleration energy is observed (open symbols in Fig. 3.11). This result suggests that, by attaching hydrogen atoms to the DBs, the latter become inactive as positron trap. As a result, the positrons implanted with acceleration energy lower than $\approx$ 5 keV will have larger diffusion length. This will lead to the observed gradual increase of the measured S-value from the one characteristic of surface positron trapping, to the value typical for positron annihilation in the bulk of the silicon substrate (this value can be found in Refs. [27][29]).

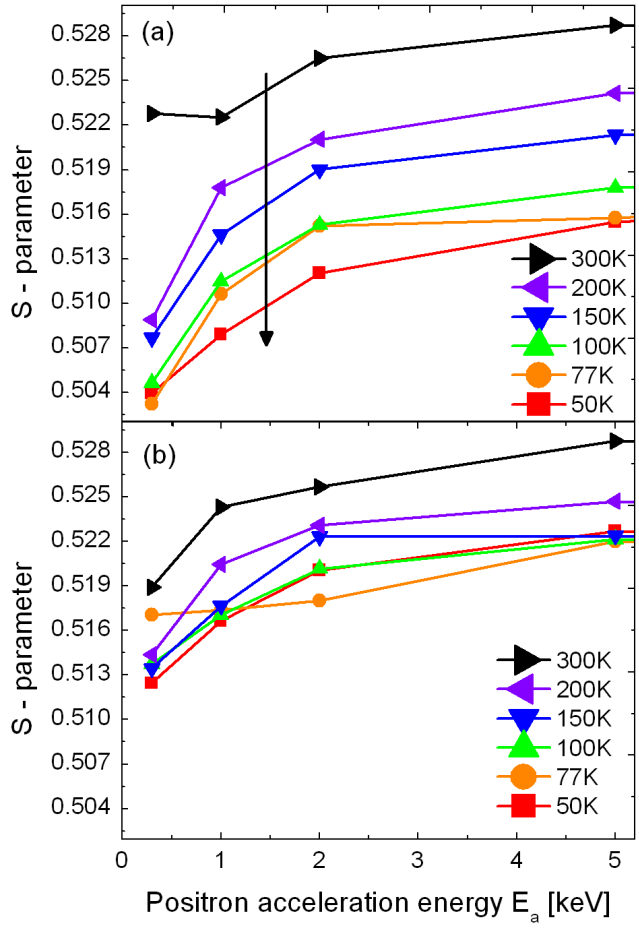


Figure 3.12: S-parameter as a function of the positron implantation energy, as measured at different temperatures (from 300 K to 50 K) on sample #4 ($Ge_{0.73}Si_{0.27}$ layer) prior- (a) and after defects passivation in H_2 (b).

Fig. 3.12(a) shows the plot of the S-parameter versus implantation energy as measured on the un-passivated sample #4 for different temperatures (ranging from 300K to 50K). It has to be noted that the difference in the absolute value of the S-parameters as compared the one reported in Fig. 3.11, is expected because two different positron beams have been used (i.e. variation on the positron generation rate at the source, on the flux diameter etc.).

As the measurement temperature is lowered from 300K to 50K a clear shift of the S-value is observed (indicated as a bold arrow in Fig. 3.12(a)). Although it is still not possible to decompose exactly the measured S-parameter into its individual components, the monotonic behavior of the S-parameter as function of acceleration energy observed at all measurement temperatures suggests that the surface of the sample always provides a smaller contribution to the overall measured S-value as the energy of positrons increases. In its turn, the observed decrease of the S-parameter measured at low acceleration energies with decreasing the measurement temperature indicates an increased surface contribution. Thus, after implantation and thermalization, positrons have a larger probability to diffuse towards the surface as the sample is cooled down, indicating a reduced e^+ trapping at the $SiGe/SiO_2$ interface.

Fig. 3.12(b) shows the results of the same experiment performed on the sample after defects passivation by annealing in H_2. As can be seen, the temperature effect is strongly reduced and S-values at all acceleration energies are more homogeneously distributed. This different behavior reflects a decreased contribution of the positron annihilation states related to the Ge DBs at the $Si_{1-x}Ge_x/SiO_2$ interface partially passivated by hydrogen.

The major conclusion from the observations is that, when the temperature decreases, positrons encounter a lower density of traps at the interfaces between $Si_{1-x}Ge_x$ and SiO_2. This suggests change in the electron occupancy of the Ge DBs with decreasing temperature.

To address the cause of this temperature-induced reduction of e^+ trapping, Fig. 3.13 shows the relative variation of the S-parameter evaluated at low acceleration energies (specifically for the points at 1 keV and 2 keV) as a function of sample temperature. The data from the un-passivated sample (filled squares and circles) exhibit a substantial linear increase with temperature and the corresponding relative increase of the S-parameter reaching $\approx 3\%$ when increasing the temperature from 50K to 300K. On the contrary, the measurements repeated after hydrogen passivation (filled triangles) exhibit a much weaker temperature dependence.

Interestingly, a similar weak increase of the S-value can be seen in the results obtained on both samples (i.e. prior- and after the passivation of defects by hydrogen) when the acceleration energy is sufficient to implant positrons deep into the Si substrate wafer (open blue triangles in Fig. 3.13). This allows one

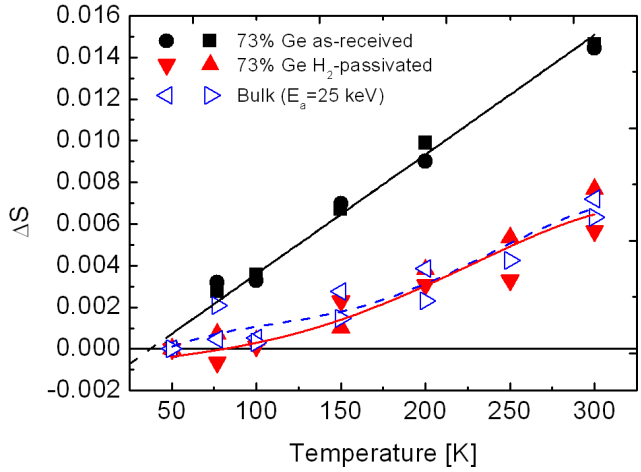


Figure 3.13: Relative variation of the S parameter measured at low implantation energies (E_a = 1 and 2 keV) on sample no. 4 ($Ge_{0.73}Si_{0.27}$ layer) prior- and after defects passivation anneal (black and red symbols, respectively) as a function of measurement temperature. For comparison, measurements obtained at high implantation energies (E_a = 25 keV, implantation in the Si bulk, open blue triangles) are also included.

to exclude the influence of additional temperature-activated positron transport phenomena in the sample, and indicates that the S shift to the higher value observed for implantation energies of 1 and 2 keV is predominantly associated with positron trapping at the sites located at the interface between $Si_{1-x}Ge_x$ and SiO_2.

Importantly, as mentioned in Section 3.1, generation of dangling bonds at the Si/SiO_2 interface is associated with sheer stress occurring during thermal oxidation process. Hence, within the explored temperature range, it is assumed that the structural stability of the samples is ensured and the number of interfacial DB defects is un-affected. Therefore, the only temperature induced effect relates to the shift of the Fermi level, which results in a change in the DBs charge state.

As mentioned, the same behavior was observed electrically (see Fig. 3.5) and thus we can correlate the PAS results to the change in the occupancy (from double, negative state, to single, neutral state) of the DB defects, which occurs when the Fermi level in the Ge_xSi_{1-x} layer crosses the defect charge transition level. The temperature-induced shift of the Fermi level away from the VB maximum will cause more defects to gain a negative charge and, since

positron trapping arises from the interaction of positrons with a negative charge, the interface-related contribution to the annihilation becomes more and more pronounced as temperature increases.

This allows one to estimate the position of the defect charge transition level by evaluating the position of the Fermi level at different temperatures which, as reported in section 2.1.3, can be quantified as:

$$E_F = E_V + \frac{E_g}{2} - kT \ln \frac{p}{n_i} \tag{3.2}$$

where the doping concentration N_A of Eq. 2.13 has been converted into free carriers (holes) concentration "p". The latter being estimated to be in the (2 - 5) $\times 10^{17} cm^{-3}$ range on the basis of Hall-effect and resistivity measurements reported in Ref. [30]. The intrinsic carrier concentration n_i has instead been calculated according to Ref. [31].

The calculations indicate that the Fermi level position in the $Ge_{0.73}Si_{0.27}$ layer varies from a maximum value of $\approx$ 0.11 eV to $\approx$ 0.01 eV above the VB maximum as the sample is cooled down from 300K to 50K. The charge transition levels of the Ge P_{b1} centers are thus inferred to lie within this energy range, refining the previously estimated (0/-) transition energy reported in Ref. [22].

Last, we report the analysis of the 1-D coincidence spectra (1-D angular coincidence Doppler broadening mode), measured on sample #4 before and after defect passivation in H_2 at room temperature and at T = 77K. In order to have a fair comparison of the data, once the Doppler spectra are obtained, they are first normalized to the total number of the observed annihilation events and then to the reference spectra. In the absence of reference spectra obtained on a pure Si/SiO_2 sample, the spectrum obtained from the as-received sample at room temperature was chosen to serve as the reference.

The results are presented in Fig. 3.14. The data show an increase in the signal intensity at high momenta when the temperature is lowered from 300K to 77K (solid and open symbols respectively). This effect could be assigned to a higher contribution of the 3d electrons of the Ge atoms, whose influence on the $e^+ - e^-$ annihilation would be greater at lower temperatures. However, such increase would be anyhow expected for a broader spectra (lower S parameter corresponds to a higher W parameter) and we have previously observed consistent variations in the S value depending on the measurement temperature which may contribute to the observed increase of events at high momentum. Thus, the conclusion regarding contribution of the Ge 3d electrons to positron annihilation would require additional support.

Therefore, whereas this results might indicate the possibility of directly sensing the atomic origin of the defect, further experiments would be needed (specifically, the data from a meaningful reference sample).

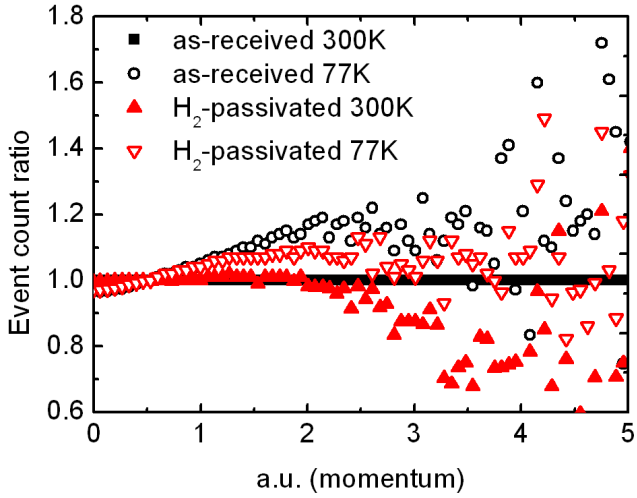


Figure 3.14: Event count ratio versus momentum plot, as obtained on sample no. 4 ($Si_{0.27}Ge_{0.73}$ layer) prior- and after defects passivation anneal (black and red symbols, respectively) at room temperature and at T = 77 K (solid and open symbols, respectively). The Doppler broadening spectra have been probed at fixed implantation energy E_a = 1 keV. Higher energies in the Doppler broadening spectra (i.e. see Fig. 2.12) correspond to annihilation events at higher momenta. Once the Doppler spectra have been obtained, all values (count of annihilation events per annihilation energy) have been normalized to the total event count and then referenced with respect to the (normalized) spectra as measured at room temperature on the as-received sample.

3.6 Conclusions

In this chapter we have studied the defectivity of $SiO_2/Si_{1-x}Ge_x/SiO_2$ heterostructures fabricated by using the Ge-condensation technique. This fabrication process is particularly interesting as it allows one to grow SiGe layers over a large wafer area.

We have shown that the residual mismatch strain represents an important factor influencing the quality of the $Si_{1-x}Ge_x/SiO_2$ interface in terms of occurring charge traps. Two major effects have been observed: First, the initial density of dangling bond defects, GeP_{b1} centers increases with increasing residual strain. Second, the efficiency of passivation of these defects by annealing in hydrogen decreases in samples with highly strained $Si_{1-x}Ge_x$ layers leaving up to 40 % of these traps resistant to the passivation.

Moreover, we have investigated the electrical activity of the Ge DB defects by means of PAS spectroscopy. Experiments in the Db mode have revealed that these defects act as efficient trapping sites for positrons, in agreement with electrical observations of a negative charge associated with each DB defect.

Further analysis of the Db lineshape parameters as a function of positron acceleration energy suggest enhanced post-thermalization diffusion of positrons towards the surface of the sample at low temperatures. This also correlates with the reduced density of positron traps in the $Si_{1-x}Ge_x$ layer. Therefore, one may conclude that the positron trapping is associated with the negative charge trapped by the Ge P_{b1} defects which is affected by the shift of the Fermi level within the semiconductor band gap. The corresponding defect charge transition from double (negatively charged) to single (neutral state) occupation is inferred to be in the energy interval of ≈ 0.1 eV near the $Si_{0.27}Ge_{0.73}$ VBT (see, as an example, Fig. 3.9).

Considering the inevitability of strain in advanced technologies, the Ge condensation technique appears not to be suitable for the fabrication of SiGe channel devices unless epitaxial overgrowth of a less defective semiconductor film is implemented.

Bibliography

[1] L. Souriau, V. Terzieva, W. Vandervorst, F. Clemente, B. Brijs, A. Moussa, M. Meuris, R. Loo, and M. Caymax, *High Ge content SGOI substrates obtained by the Ge condensation technique: A template for growth of strained epitaxial Ge* Thin Solid Films, **517**(1), 23 (2008)

[2] L. Souriau, T. Nguyen, E. Augendre, R. Loo, V. Terzieva, M. Caymax, S. Cristoloveanu, M. Meuris, and W. Vandervorst *High-hole-mobility Silicon Germanium on Insulator substrates with high crystalline quality obtained by the Germanium Condensation Technique* J. Electrochem. Soc., **156**, 208 (2009)

[3] R.C. Newman *Defects in silicon* Rep. Prog. Phys., **45** (1982)

[4] A. Stesmans *Structural relaxation of P_b defects at the (111)Si/SiO_2 interface as a function of oxidation temperature: The P_b-generation-stress relationship* Phys. Rev. B, **48**, 2418 (1993)

[5] C. R. Helms, and E. H. Poindexter *The silicon-silicon dioxide system: Its microstructure and imperfections* Rep. Prog. Phys., **57**, 791 (1994)

[6] E. H. Poindexter *MOS interface states: overview and physicochemical perspective* Semicond. Sci. Technol., **4**, 961 (1989)

[7] A. Stesmans, and V. V. Afanas'ev *Electrical activity of interfacial paramagnetic defects in thermal (100) Si/SiO_2* Phys. Rev. B, **57**, 10030 (1998)

[8] N.H. Thoan, K. Keunen, V.V. Afanas'ev, and A. Stesmans *Interface state energy distribution and P_b defects at (110)Si/SiO_2 interfaces: comparison to (111) and (100) silicon orientations* J. Appl. Phys., **109**, 013710 (2011)

[9] A. Stesmans *Interaction of P_b defects at the (111)Si/SiO_2 interface with molecular hydrogen: Simultaneous action of passivation and dissociation* J. Appl. Phys., **88**, 489 (2000)

[10] A. Stesmans *Influence of interface relaxation on passivation kinetics in H_2 of coordination P_b defects at the (111)Si/SiO_2 interface revealed by electron spin resonance* J. Appl. Phys., **92**, 1317 (2002)

[11] A. Stesmans and V. Afanas'ev *Si dangling-bond defects at the interface of (100)Si with ultrathin HfO_2* Appl. Phys. Lett., **82**(23), 4074 (2003)

[12] A. Stesmans and V.V. Afanas'ev *Si dangling-bond-type defects at the interface of (100)Si with ultrathin layers of SiO_x, Al_2O_3, and ZrO_2* Appl. Phys. Lett., **80**, 1957 (2002)

[13] K. Clemer, A. Stesmans, V.V. Afanas'ev, L.F. Edge and D.G. Schlom *Paramagnetic point defects in (100)Si/$LaAlO_3$ structures: Nature and stability of the interface* J. Appl. Phys., **102**, 034516 (2007)

[14] V. Afanas'ev, Y.G. Fedorenko, and A. Stesmans *Interface traps and dangling-bond defects in (100)Ge/HfO_2* Appl. Phys. Lett. **87**, 032107 (2005)

[15] F. Bellenger, M. Houssa, A. Delabie, V. Afanasiev, and T. Conard *Passivation of Ge(100)/GeO_2/high-k gate stacks using thermal oxide treatments* J. Electrochem. Soc. **155**, 33 (2008)

[16] C.G. Van de Walle, M. Choi, J.R. Weber, J.L. Lyons, and A. Janotti *Defects at the Ge/oxide and III-V/oxide itnerfaces* Microelectron. Eng. **109**, 211 (2013)

[17] S. Baldovino, A. Molle, and M. Fanciulli, *Evidence of dangling bond electrical activity at the Ge/oxide interface* Appl. Phys. Lett. **93**(24), 242105 (2008)

[18] M.E. Zvanut, W.E. Carlos, M.E. Twigg, R.E. Stahlbush, and D.J. Godbey *Observation of a Trivalent Ge Defect in Oxygen Implanted SiGe Alloys* Mater. Sci. Forum **83**, 1493 (1992)

[19] S. Lebib, M. Schoisswohl, J.L. Cantin, and H.J. Von Bardeleben *SiGe/SiGeO$_2$ interface defects* Thin Solid Films, **294**, 242 (1997)

[20] A. Stesmans, P. Somers, and V. Afanas'ev, *Nontrigonal Ge dangling bond interface defect in condensation-grown (100)Si$_{1-x}$Ge$_x$/SiO$_2$* Phys. Rev. B **79**(19), 195301 (2009)

[21] K. Sankaran, G. Pourtois, M. Houssa, A. Stesmans, M. Caymax and M.M. Heyns *First-principles investigation of the electron spin resonance parameters of germanium interfacial dangling bond centers* Appl. Phys. Lett. **94**, 184103 (2009)

[22] V. Afanas'ev, M. Houssa, A. Stesmans, L. Souriau, R. Loo, and M. Meuris *Electronic properties of Ge dangling bond centers at Si$_{1-x}$Ge$_x$/SiO$_2$ interfaces* Appl. Phys. Lett., **95**, 222106 (2009)

[23] M. Houssa, G. Pourtois, M. Meuris, M.M. Heyns, V. Afanasev, and A. Stesmans *Experimental and theoretical investigation of defects at (100)Si$_{1-x}$Ge$_x$/oxide interfaces* Microelectron. Eng., **88**, 383 (2011)

[24] A. Stesmans, T. Nguyen Hoang and V.V. Afanas'ev *Hydrogen interaction kinetics of Ge dangling bonds at the Si$_{0.25}$Ge$_{0.75}$/SiO$_2$ interface* J. Appl. Phys. **116**, 044501 (2014)

[25] N.H. Thoan, A. Stesmans, A.P.D. Nguyen, K. Keunen, and V. Afanasev *Chemical kinetics of the hydrogen-GeP$_{b1}$ defect interaction at the (100)Ge$_x$Si$_{1-x}$/SiO$_2$ interface* J. Vac. Sci. Technol. B, **31**(1), 010603 (2013)

[26] B. Vincent, R. Loo, W. Vandervorst, J. Delmotte, B. Douhard, V.K. Valev, M. Vanbel, T. Verbiest, J. Rip, B. Brijs, T. Conard, C. Claypool, S. Takeuchi, S. Zaima, J. Mitard, B. De Jaeger, J. Dekoster, and M. Caymax, *Si passivation for Ge pMOSFETs: Impact of Si cap growth conditions* Solid. State. Electron., **60**(1), 116 (2011)

[27] F. Tuomisto, and I. Makkonen *Defect identification in semiconductors with positron annihilation: Experiment and Theory* Rev. Mod. Phys., **85**(4), 1583 (2013)

[28] J. Slotte and F. Tuomisto *Advances in positron annihilation spectroscopy of Si, Ge and their alloys* Mat. Sci. Semicon. Proc., **5**, 669 (2012)

[29] S. Kilpelainen, J. Kujala, F. Tuomisto, J. Slotte, Y.W. Lu, and A. Nylandsted Larsen *Si nanoparticle interfaces in Si/SiO$_2$ solar cell materials* J. Appl. Phys., **114**(16), 164316 (2013)

[30] N. Hirashita, Y. Moriyama, S. Nakaharai, T. Irisawa, N. Sugiyama and S. Takagi *Deformation induced holes in Ge-rich SiGe-on-insulator and Ge-on-insulator substrates fabricates by Ge condensation process* Appl. Phys. Express **1**, 101401 (2008)

[31] F. Schaffler *Properties in advanced semiconductor materials: GaN, AlN, InN, BN, SiC, SiGe* John Wiley and Sons, New York (2001)

Chapter 4

Defect density reduction in Si-passivated epi-SiGe channel devices with HfO_2 insulator

The large mismatch between the Ge and Si crystal lattices implies that a certain amount of strain is always present in the stack if growing a Ge layer on a Si substrate.

Moreover, as discussed in the introduction, since 2003 strain has been **intentionally** applied to Si channels in order to enhance charge carrier mobilities. Similar improvements are also expected to occur, if properly using strain, in Ge-based channels. However, the correlation between residual strain and generation of interface defects demonstrated in the previous chapter raises questions regarding the feasibility of this approach.

As the fabrication of SiGe layers by the Ge-condensation technique leads to high levels of residual strain, in this chapter we explore defects at interfaces of epitaxially grown SiGe layers on silicon. Whereas pseudomorphic growth implies the presence of considerable strain, Si-passivated epi-grown SiGe pMOSFETs have been repeatedly shown to deliver a superior reliability as compared to the pure-Si reference devices [1]. In order to gain further insight on the physical mechanism of this reliability improvement, we characterized Si/SiGe/Si/HfO_2 heterostructures processed in the same way as the MOSFETs examined in Ref. [1].

The major challenge of this work is related to the presence of a *Quantum*

well for holes (see Fig. 1.3) that provides dominant AC response in the electrical measurements. As a result, the electrical "fingerprint" of defects become undetectable if analyzing MOS capacitors. Nevertheless, the defect densities still can be determined by ESR measurements.

ESR study of defects in samples with different channel compositions and passivation schemes, allowed us to reach two main conclusions: First, it appears that the dangling bonds of Si atoms (P_b-centers) are (probably) generated at the back interface between the Si substrate and the SiGe QW. Second, a reduction of the Si DB defect density is seen to correlate with the ability of Ge atoms to out-diffuse from the channel region. Remarkably, it is found that a critical Ge concentration of about ≈ 28 % correlates to a reduction of Si DB density below the detection limit ($\approx 10^{11} cm^{-2}$), in agreement with the behavior reported in the previous chapter for the condensation-grown $Si_{1-x}Ge_x/SiO_2$ ($x > 28\%$) heterostructures, where **no measurable density of Si DBs** was found as well.

4.1 Samples description, preparation, and characterization details

In order to be able to compare the ESR results obtained here with the previously published electrical data, the studied samples have been fabricated following the full state-of-the-art metal-gate stack processing [2], [3] but without lithographic patterning and source / drain implants.

Starting from 300mm (100) Si blanket wafers, a pre-epi clean and etchback of Si is carried on, and a Si buffer of 2 nm is grown at 500 $^\circ C$ with SiH_4 as precursor to ensure a high quality Si starting surface. Epitaxial growth of $Si_{1-x}Ge_x$ layers was carried out from SiH_4 and GeH_4 precursors. Different temperatures have been employed during this process to tune the final Ge concentration in the layer, which have been chosen to be $x_{Ge} = 0.25$, 0.45, and 0.55. The final thickness of the SiGe layer also differs between the samples T_{SiGe} = 10, 7 and 5 nm which corresponds to the pseudomorphic growth. The gate stack formation started from a Si cap of varying thickness (T_{SiCap} = 1 to 3 nm) grown at 450 $^\circ C$ by using SiH_4 as precursor, followed by the IMEC cleaning process. The latter results in formation of a $\approx$ 1 nm thick SiO_2 interfacial layer. Finally, 1.8 nm HfO_2 is deposited through ALD process. For comparison, a reference sample was also produced by depositing 5 nm PECVD SiO_2.

On top of the oxide insulator, metal electrode consisting of 2 nm of TiN, 50 nm phosphorous doped polycrystalline Si and NiSi, was deposited. To complete the metal gate fabrication, a spike anneal at 1000 $^\circ C$ or 1035 $^\circ C$ for 1.5 sec was performed. This process serves the double purpose of activation

anneal for the poly-Si dopants and for the oxygen scavenging, enabled by the TiN/Si stack in order to reduce the SiO_2 interlayer and lower the EOT of the overall gate stack to ≈ 0.6 nm target.

The final device cross-section and band diagrams were already shown in Chapter 1, Fig. 1.3(a),(b). Table 4.1 summarizes the studied $Si_{1-X}Ge_X$ channel compositions, passivation schemes, as well as the insulating layer composition and thickness. More details on the processes described above can be found elsewhere [2], [3]. Finally, MOS structures were defined by wet chemical etching of the top metal gate stack using an organic mask (details of the etching recipe will be given later).

Table 4.1: Structure of the studied samples and the density of the observed Si P_{b0} defects. For each sample a code is indicated.

	Channel	Passivation	Insulator	$[P_{bo}]$ (cm^{-2})
S01	Si	None	1.8nm ALD HfO_2	$(3.8 \pm 0.5) \cdot 10^{12}$
S02	5nm $Si_{0.45}Ge_{0.55}$	1nm Si	5nm PECVD SiO_2	$(0.8 \pm 0.1) \cdot 10^{12}$
S03	10nm $Si_{0.75}Ge_{0.25}$	None	1.8nm ALD HfO_2	$(0.9 \pm 0.1) \cdot 10^{12}$
S04	5nm $Si_{0.45}Ge_{0.55}$	1nm Si	1.8nm ALD HfO_2	$(0.9 \pm 0.1) \cdot 10^{12}$
S05	7nm $Si_{0.55}Ge_{0.45}$	1nm Si	1.8nm ALD HfO_2	$< 8 \cdot 10^{10}$
S06	5nm $Si_{0.45}Ge_{0.55}$	3nm Si	1.8nm ALD HfO_2	$< 8 \cdot 10^{10}$
S07	7nm $Si_{0.45}Ge_{0.55}$	1nm Si	1.8nm ALD HfO_2	$(1.8 \pm 0.5) \cdot 10^{10}$
S08	7nm $Si_{0.45}Ge_{0.55}$	3nm Si	1.8nm ALD HfO_2	$< 8 \cdot 10^{10}$

Electrical characterization of interface traps is hampered by the large AC response of the $Si_{1-x}Ge_x$ QW. As an example, Fig. 4.1 shows the CV curves measured at room temperature using the probe signal frequencies from 400 Hz to 1 MHz on sample S04.

As can be seen from Fig. 4.1, at the onset of depletion trapping and emission of holes in the QW gives rise to an electrical response which is not considered in the model of a classical MOS structure with uniform semiconductor electrode (see Fig. 2.3(c)). This response makes impossible detection of the signal stemming from interface states. As a result, the equivalent model shown in Fig. 2.4, upon which the CV and GV D_{IT} extraction techniques are based, becomes inapplicable.

An alternative model incorporating the response of the QW has been proposed by Takagi *et. al.* [4] with the intent of estimating the valence band discontinuity that constitutes the QW itself (ΔE_V in Fig. 1.3). Interestingly, considering that the QW response can be be several orders of magnitude larger than the signal from interface traps, the latter can be neglected, and the new model is still analogous to the one presented in Fig. 2.4 (see. Fig. 2(a),(b) in Ref. [4] for comparison).

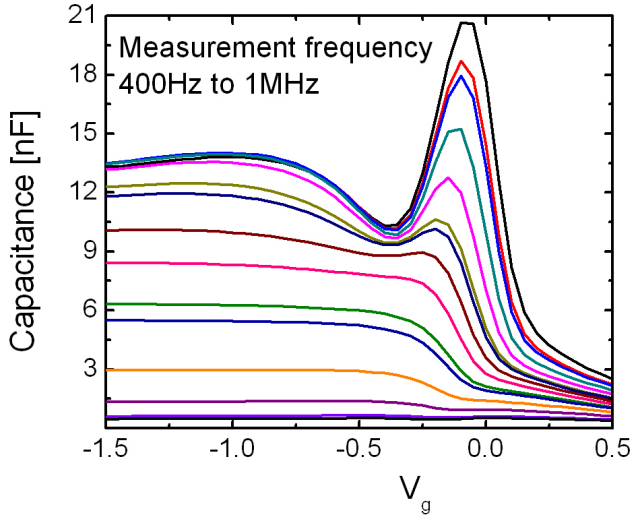


Figure 4.1: CV curves as measured on sample S04 at room temperature at frequencies from 400 Hz to 1 MHz. The response of the QW is seen as the large peak in capacitance in the depletion region.

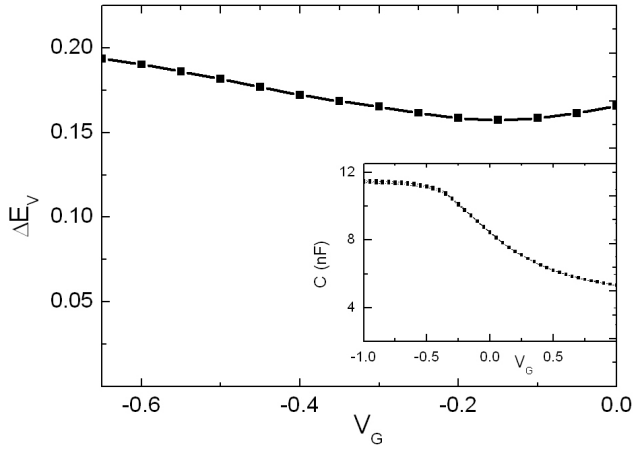


Figure 4.2: Valence band discontinuity ΔE_V estimated as a function of gate bias. The inset shows the CV curve measured at 100 kHz in liquid nitrogen bath (T = 77K) on sample S04.

Fig. 4.2 shows the valence band discontinuity between Si and the $Si_{1-x}Ge_x$ QW as estimated as a function of gate bias by using the methodology proposed in Ref. [4]. The inset depicts the CV curve as measured at 100 kHz at the temperature of 77K on sample S04. This temperature was chosen as it shifts the Fermi energy closer to the VBT and enhances the response of the QW well.

Within the bias range under consideration, one can estimate $\Delta E_V = 0.17 \pm 0.03$ eV, in line with the expectations: Since most of the band gap narrowing when going from Si to Ge occurs on the valence band side [5], the difference between the band gap of Si and $Si_{0.45}Ge_{0.55}$ ($E_g(Si) = 1.12$ eV and $E_g(Si_{0.45}Ge_{0.55} = 0.97$ eV as from Ref. [6], respectively) is approximately $\Delta E_V = 0.15$ eV, which is consistent experimental value inferred from 77K CV measurements.

Therefore, the QW is confirmed to provide the dominant contribution to the AC response of the studied samples. As a consequence, quantification of the defect densities was carried out by means of electron spin resonance spectroscopy.

The presence of metallic gate layers is detrimental to the ESR, as it impedes the penetration of microwaves deep into the sample and induces microwave losses. As a result, removal of the gate stack multilayer was mandatory in order to enable observation of ESR spectra.

To accomplish this goal, the multilayer gate stack was removed by using a series of selective wet-etchings in order to avoid damaging the interface between the semiconductor channel and the oxide insulator. Starting from a HNO_3 and HCl 1:1 aqueous solution to remove the NiSi top layer, a 25% solution of tetra-methyl ammonium hydroxide (TMAH) was used to selectively etch the poly-Si over the TiN layer. Finally, an aqueous peroxide (H_2O_2) solution at 70 $^\circ C$ was used to remove the TiN layer selectively over the HfO_2 insulator. Surface cleaning, consisting of water rinse and a short (30 sec) aqueous HF [HF (49%): H_2O 1:9] solution deep, were performed in between each step to eliminate surface oxides.

Next, samples were thinned down to ≈ 150 μm by etching the Si substrate from the backside using CP4 etchant. Slices of $\approx 2 \times 9 mm^2$ area were cut from these structures. The cutting damage (from a diamond saw) was removed through chemical wet-etching using the same CP4 ($HF:HNO_3:CH_3COOH$ solution) etch.

Prior to each ESR experiment, all samples have been exposed for 600 sec to 10 eV photons from a Kr-discharge lamp through a MgF_2 window. Photons of such energies are able to break Si - H bonds thus exposing the present Si DBs by making them available for the ESR analysis.

Conventional cw first derivative absorption (dPμr/dB, where Pμr is the reflected microwave power) K-band (≈ 20.4 GHz) ESR spectra were measured

in the adiabatic mode at ≈ 4.3 - 4.5 K. Signal averaging was routinely applied (50 - 100 scans) to enhance the signal to noise ratio. A calibrated co-mounted Si:P reference sample [electron spin S = $\frac{1}{2}$; g(4.2 K) = 1.99869 ± 0.00002] was used for g factor and defect (spin) density determination, where the latter was carried out through double numerical integration of observed adsorpion derivative signals. The attained absolute and relative accuracies are estimated at 20% and ≤ 10% respectively. The field angular dependence of signals was studied for B rotating in the (011) plane for (100) Si/SiGe/Si/HfO_2 slices, with φ_B (angle of B with the interface normal) varying over ≈ 90°.

4.2 Reduction of Si P_{b0} centers in Si-passivated SiGe MOS devices caused by Ge out-diffusion

In section 1.4 we have given an overview of the Bias Temperature Instability problem affecting electronic devices. In particular, the effect of negative BTI affecting pMOSFET devices is especially detrimental, as the defects responsible for the V_T shift also degrade the channel mobility, which value for p-type devices is already intrinsically lower than for n-channel ones.

Nevertheless, several studies [1] [7] [8] indicated that pMOSFET HKMG Si-capped SiGe channel devices exhibit a better reliability as compared to the pure Si-channel devices, while mantaining substantially higher hole mobilities. Whereas several models have been advanced to explain this enhanced performance, the reduced instability in its *permanent* component is commonly attributed to an interfacial defect density reduction. However, the root cause of this reduced interface defectivity is still unclear.

A previous study on Si-channel samples with **the same** HKMG stack as in Ref.[8], revealed that high temperature processing (oxygen scavenging anneal, $T > 1000\ ^\circ C$) required to eliminate interfacial SiO_X and achieve low EOT also causes severe interface degradation in terms of defect generation [9].

It thus seems that the presence of Ge atoms may have a critical impact on the observed improvement of the reliability of the devices.

Fig. 4.3 shows the first-derivative absorption ESR spectra as measured on the sample with a $Si_{0.45}Ge_{0.55}$-channel passivated by 1 nm Si cap (S04 in Table 4.1), as compared to the Si-channel control sample (S01 in Table 4.1). Both samples exhibit a signal with characteristic g value of 2.0060, typical of Si P_{b0} centers. Similar signals have also been detected when performing ESR analysis of all samples in the available set and the resolved defect densities are summarized in the right column in Table 4.1 (the case for samples S05, S06 and S08 will be discussed in more detail later).

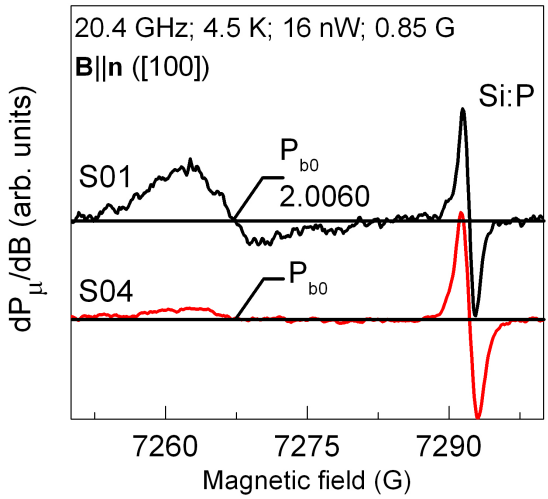


Figure 4.3: First derivative-absorption K-band ESR spectra as measured for B||n ([100] interface normal) on Si-passivated $Si_{0.45}Ge_{0.55}$ channel sample (S04) and the pure Si channel sample (S01). The Si DB signal P_{b0} at g = 2.0060 and the Si:P marker are indicated for both samples.

Fig. 4.4 compares the Si P_{b0} defects densities as evaluated on samples S02, S03 and S04. The schematic cross-section of the samples is also shown in the figure. A first noteworthy comparison can be done between samples S02 and S04. Though both samples were processed with a 5 nm $Si_{0.45}Ge_{0.55}$ channel layer and passivated by a 1 nm Si capping layer, they differ in the top gate oxide composition: 5 nm PECVD SiO_2 in sample S02 and 1.8 nm ALD HfO_2 in sample S04, respectively. As can be seen from Fig. 4.4 (as well as from Table 4.1), the Si P_{b0} defect density is not significantly affected, suggesting that the insulator processing has no substantial impact on the defect generation.

Next, observation of nearly the same Si DB density in sample S03 raises an important question regarding the spatial location of the revealed interfacial defect. The presence of Si P_{b0} densities of about $0.9 \cdot 10^{12} cm^{-2}$ in both the Si/10 nm $Si_{0.75}Ge_{0.25}/HfO_2$ and Si/5 nm $Si_{0.45}Ge_{0.55}/Si/HfO_2$ structures, and of about $0.8 \cdot 10^{12} cm^{-2}$ in the Si/5 nm $Si_{0.45}Ge_{0.55}/SiO_2$ structure, seems to suggest that these defects are located at the interface between the Si substrate and the SiGe layers rather than at the Si/oxide interface.

It is known that the generation of P_b centers in Si/SiO_2 systems is driven by interfacial stress arising from the $Si\text{-}SiO_2$ lattice mismatch (a factor of ≈ 2.2 difference between the molar volume of Si and of SiO_2 [10]). In our

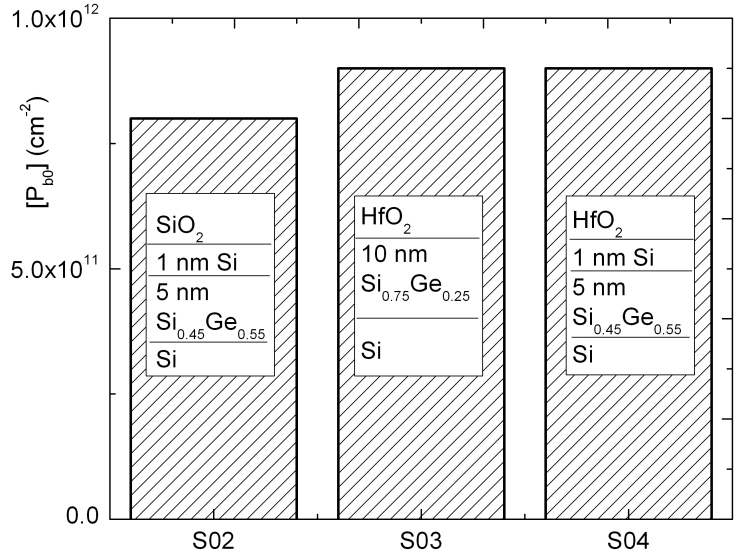


Figure 4.4: Densities of Si P_{b0} centers as resolved on samples S02, S03 and S04. The composition of each sample is schematically indicated for comparison.

case, similar levels of residual interfacial stress among the analyzed samples may be encountered at the bottom interface between the Si substrate and the pseudomorphic SiGe layers, rather than at the top interfaces.

Fig. 4.5 summarizes the results obtained on all the samples with a top 1.8 nm ALD-grown HfO_2 insulator. Here, the density of Si P_{b0} centers is shown as a function of the total areal density of Ge atoms in the $Si_{1-x}Ge_x$ layer of each sample. The introduction of Ge is seen to dramatically improve the interfaces quality.

While in the case of the pure Si channel in the control sample S01 a Si DB density of about $3.8 \cdot 10^{12} cm^{-2}$ is found, the defect density on the Ge-containing samples is much lower: $1.8 \cdot 10^{12} cm^{-2}$ in sample S07, and even lies below the detection limit in samples S05, S06 and S08.

Though the samples under investigation have been fabricated with different Ge concentrations and with different thicknesses of the SiGe layer and thickness of the Si capping layer, a direct comparison can be done between P_{b0} densities found in samples S04 and S06, as well as between samples S07 and S08. These samples were fabricated with a 5 nm and 7 nm $Si_{0.45}Ge_{0.55}$ layer, respectively, but were provided with a different Si passivation layers. In particular, on samples S04 and S07 only a 1nm thick Si cap was deposited,

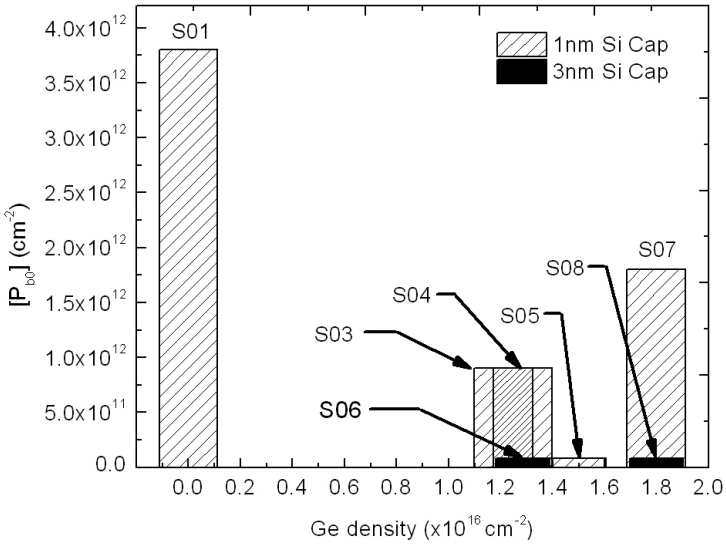


Figure 4.5: Densities of Si P_{b0} centers, as inferred in all samples provided with 1.8 nm ALD-grown HfO_2, as a function of the density of Ge atoms contained in each sample ($d_{Ge} = Atomic_{Density} \times Ge_{fraction} \times Thickness_{SiGe\ layer}$)

while on samples S06 and S08 a thicker 3 nm capping was used.

While the samples with a thinner cap (S04 and S07) exhibited a Si DB density of $0.9 \cdot 10^{12} cm^{-2}$ and $1.8 \cdot 10^{12} cm^{-2}$, respectively, the ESR spectra measured on the samples with a thicker Si cap (not shown) presented no evidence of a P_b-like line, indicating the P_{b0} densities to be below detection limit ($< 8 \cdot 10^{10} cm^{-2}$).

Although the physical mechanism behind the defect density reduction is not clear, the experimental results presented in this and in the previous chapter indicate that the presence of a certain amount of Ge ($\geq$ 28 %) in alloy with Si, allows to suppress the generation of Si dangling bond defects. At the same time, no evidence of Ge DB centers has been found for x < 55 %.

Tentatively, the data of Fig. 4.5 can be explained by considering the amount of Ge diffusing out of the SiGe layer and incorporated into near-interface silicon layer. Once the concentration of Ge in Si becomes sufficient to suppress the DB formation, as it has been observed for the condensation-grown $Si_{1-x}Ge_x$ ($x < 0.55$), these defects disappear.

In particular two main factors should be taken into account. First, segregation of Ge atoms at the surface of the Si capping layer is known to happen in Si-passivated Ge devices processed with the same HKMG stack as

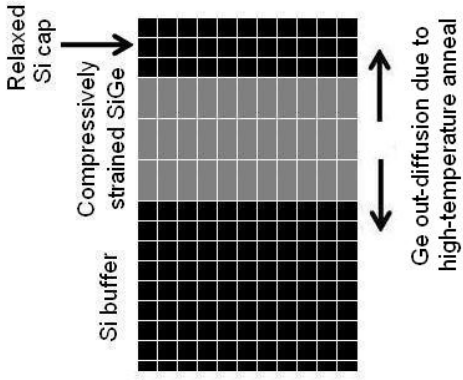


Figure 4.6: Sketch illustrating the composition of the as-fabricated Si/SiGe/Si heterostructure. During the grow of the Si capping layer, Ge segregation at its surface induces strain relaxation at the top SiGe/Si cap interface. Subsequent thermal treatment (oxygen scavenging anneal) induces further Ge out-diffusion towards the top and bottom interfaces. In the figure, black indicates pure Si, and grey SiGe. The amount of Ge out-diffusing depends on the thicknesses of the SiGe layer and Si capping layers, as well as on the Ge concentration in the SiGe layer.

the samples used in this work [11], [12]. Importantly, as shown by Vincent et al. in Ref.[11], this phenomenon is seen to occur already **during** the Si passivation layer growth. It is thus foreseeable that the high-temperature oxygen scavenging anneal would induce further Ge out-diffusion. Then, because of Ge loss, less germanium "doping" of Si substrate is expected. The sketch in Fig. 4.6 uses shades of black and grey to illustrate the composition of the as-fabricated Si/SiGe/Si heterostructure. The oxygen scavenging anneal performed during the fabrication of the gate stack induces Ge out-diffusion towards the top and bottom interfaces.

Second, residual strain in SiGe layers is known to enhance out-diffusion of Ge atoms upon annealing [13], [14]. The same studies also reported that the exhaustion of the out-diffusion phenomena coincided with relaxation of the strain in the SiGe layer.

SiGe layers with higher levels of residual strain **at the moment** the oxygen scavenging anneal, would see enhanced Ge out-diffusion and result with a lower Si DBs defect density. On the contrary, samples whose residual strain

is partially relieved as a consequence of the Ge segregation occurring during the Si capping growth will see reduced Ge out-diffusion into the Si substrate and hence result in a higher defect density.

This picture would explain the results obtained on samples processed with a thicker (3 nm) Si passivation layer which are seen to yield the lowest defect density (Fig. 4.5) by limiting the Ge segregation and the associated strain relaxation. A more uniform strain configuration across the SiGe layer would thus favor out-diffusion of Ge atoms also towards the bottom interface between the Si substrate and the SiGe layer itself, hence making more likely to reach Ge concentrations which would be sufficient to reduce the Si DB densities to below $10^{11} cm^{-2}$.

In addition, strain in SiGe layers is expected to depend strongly on the Ge concentration, but has a less pronounced dependence on the SiGe layer thickness [15], [16]. This difference might explain the different defect densities found in samples S04, S05 and S07.

4.3 Conclusions

In this chapter we have presented an electron spin resonance study of $Si/Si_{1-x}Ge_x/Si/HfO_2$ structures provided with a metal gate stack. Different Ge concentrations ($0.25 < x < 0.55$), thicknesses of the SiGe channel layer (T_{SiGe} = 10 nm, 7 nm, 5 nm) and thicknesses of the Si passivation layer ($T_{Si\ Cap}$ = 1 nm , 3 nm) have been explored.

Contrarily to what was observed in the case of the condensation-grown samples of Chapter 3, we have revealed the presence of Si P_{b0} dangling bond defects located at the interfaces between the Si substrate and the SiGe channel.

Importantly, their density is seen to be strongly reduced as compared to a pure Si-channel control sample processed with the same gate stack technology, even falling below the ESR detection limit when a thick passivation layer is used.

We suggest a correlation between such decreased defect density and out-diffusion of Ge atoms from the SiGe channel layer into the Si substrate caused by post-deposition anneal. These results might help to explain the reduced voltage instability, i.e. better NBTI response, reported on the MOSFETs with identical gate stack.

Overall, chapters 3 and 4 have been devoted to the study of SiGe technologies with a Ge concentration up to 93 %. The next chapter will be

dedicated to the study of pure-Ge samples.

Bibliography

[1] J. Franco, B. Kaczer, P.J. Roussel, J. Mitard, M. Cho, L. Witters, T. Grasser, and G. Groeseneken *SiGe channel technology: Superior reliability toward ultra-thin EOT devices. Part I: NBTI* IEEE Trans. Electron. Dev., textit60(1), (2013)

[2] L. Ragnarsson, Z. Li, J. Tseng, T. Schram, E. Rohr, M.J. Cho, T. Kauerauf, T. Conard, Y. Okuno, B. Parvais, P. Absil, S. Biesemans, and T.Y. Hoffmann, *Ultra low-EOT (5 A) gate-first and gate-last high performance CMOS achieved by gate-electrode optimization* IEEE Proc. IEDM, 28.5.1 (2009)

[3] G. Hellings, L. Witters, R. Krom, J. Mitard, A. Hikavyy, R. Loo, A. Schulze, G. Eneman, C. Kerner, J. Franco, T. Chiarella, S. Takeoka, W. Vandervorst, P. Absil, S. Biesemans, M. Heyns, K. De Meyer, M. Meuris, and T. Hoffmann, *Implant-Free SiGe Quantum Well pFET: A novel, highly scalable and low thermal budget device, featuring raised source/drain and high-mobility channel* IEEE Proc. IEDM, 10.4.1 (2010)

[4] S. Takagi, J. Hoyt, K. Rim, W. Jeffrey, and J. Gibbons *Evaluation of the valence band discontinuity of* $Si/Si_{1-X}Ge_X/Si$ *heterostructures by application of admittance spectroscopy to MOS capacitors* IEEE Trans. Electron Dev., **45**(2), 494 (1998)

[5] V. Afanas'ev, A. Stesmans, L. Souriau, R. Loo, and M. Meuris *Valence band energy in confined* $Si_{1-X}GeX$ $(0.28 < X < 0.93)$ *layers* Appl. Phys. Lett., **94**(17), 2106, (2009)

[6] L .Yang, J. Watling, R. Wilkins, M. Boriçi, J. Barker, A. Asenov, and S. Roy *Si/SiGe heterostructure parameters for device simulations* Semicond. Sci. and Tech., **19**(10), 1174 (2004)

[7] J. Franco, B. Kaczer, J. Mitard, M. Toledano-Luque, G. Eneman, P.J. Roussel, M. Cho, T. Kauerauf, L. Witters, A. Hikavyy, G. Hellings, L. Ragnarsson, N. Horiguchi, T. Grasser, M. Heyns, and G. Groeseneken, *Reliability of SiGe channel MOS* ECS Trans., textbf50(9), 177 (2013)

[8] J. Franco, B. Kaczer, G. Eneman, M. Cho, J. Mitard, L. Witters, T.Y. Hoffmann, G. Groeseneken, F. Crupi, and T. Grasser, *On the Recoverable and Permanent Components of Hot Carrier and NBTI in Si pMOSFETs and their Implications in* $Si_{0.45}Ge_{0.55}$ *pMOSFETs* IEEE Proc. IRPS, 624 (2011)

[9] F. Cerbu, A.P.D. Nguyen, J. Kepa, V.V. Afanas'ev, and A. Stesmans, *Generation of Si dangling bond defects at Si/insulator interfaces induced by oxygen scavenging* Phys. Status Solidi(B), **4**, 1 (2014)

[10] A. Stesmans *Structural relaxation of P_b defects at the (111)Si/SiO_2 interface as a function of oxidation temperature: The P_b-generation-stress relationship* Phys. Rev. B, **48**, 2418 (1993)

[11] B. Vincent, R. Loo, W. Vandervorst, J. Delmotte, B. Douhard, V.K. Valev, M. Vanbel, T. Verbiest, J. Rip, B. Brijs, T. Conard, C. Claypool, S. Takeuchi, S. Zaima, J. Mitard, B. De Jaeger, J. Dekoster, and M. Caymax, *Si passivation for Ge pMOSFETs: Impact of Si cap growth conditions* Solid. State. Electron., **60**(1), 116 (2011)

[12] M. Heyns, C. Adelmann, G. Brammertz, D. Brunco, M. Caymax, B. De Jaeger, A. Delabie, G. Eneman, M. Houssa, D. Lin, K. Martens, C. Merckling, M. Meuris, J. Mittard, J. Penaud, G. Pourtois, M. Scarrozza, E. Simoen, S. Sioncke, and W.E. Wang, *Ge and III/V devices for advanced CMOS* 2009 10th Int. Conf. Ultim. Integr. Silicon, 83 (2009)

[13] Y.S. Lim, J.Y. Lee, H.S. Kim, and D.W. Moon, *Strain-induced anisotropic Ge diffusion in SiGe/Si superlattices* Appl. Phys. Lett., **80**(14), 2481 (2002)

[14] Y.S. Lim, J.S. Jeong, J.Y. Lee, H.S. Kim, H.K. Shon, H.K. Kim, and D.W. Moon, *Dry thermal oxidation of a graded SiGe layer* Appl. Phys. Lett., **79**(22), 3606 (2001)

[15] L. Souriau, V. Terzieva, W. Vandervorst, F. Clemente, B. Brijs, A. Moussa, M. Meuris, R. Loo, and M. Caymax, *High Ge content SGOI substrates obtained by the Ge condensation technique: A template for growth of strained epitaxial Ge* Thin Solid Films, **517**(1), 23 (2008)

[16] L. Souriau, T. Nguyen, E. Augendre, R. Loo, V. Terzieva, M. Caymax, S. Cristoloveanu, M. Meuris, and W. Vandervorst, *High-Hole-Mobility Silicon Germanium on Insulator substrates with high crystalline quality obtained by the Germanium* J. Electrochem. Soc., **156**(3), 208 (2009)

Chapter 5

Ge / oxide interface traps: Fast versus slow states

In the previous chapters, interface defects pertaining to two different technologies employing SiGe alloys as channel material have been explored. Charge trapping by these defects are shown to be significant factors determining the electrical degradation of the SiGe/oxide interfaces.

However, the long standing association of interface traps with semiconductor dangling bond defects is severely challenged in the case of Ge/oxide interfaces. Remarkably, despite high densities of interface traps being reported on the basis of electrical characterization results, no comparable density of paramagnetic defects was ever found in the pure Ge/oxide structures. At the same time, the literature results suggest that such high trap densities may be related to defects located within the insulating oxide stack [1][2][3][4].

In order to gain further insight into this matter, a reliable assessment of the interface trap density and their energy distribution is essential. Unfortunately, the traditionally used electrical characterization techniques developed for Si/SiO_2 interface characterization fall short when analyzing Ge/oxide entities. This interface characterization challenge is addessed in this chapter: D_{IT} energy distributions will be evaluated in Ge/Sc-doped GeO_2/HfO_2 structures by means of the Saturation surface PhotoVoltage (SPV) as well as by using more conventional capacitance and admittance-based characterization techniques. Since the SPV represents a nearly quasi-static method, the comparison between these two trap evaluation techniques confirms that a large part of traps at the Ge/oxide interfaces are *slow* charge trapping defects escaping detection by the conventional AC techniques.

Finally, the SPV analysis will be extended to a number of Ge interfaces fabricated by using different Ge passivation schemes.

5.1 Limitations of conventional trap characterization techniques for high-mobility semiconductor / high-k insulator stacks

As described in Chapter 2, the most widely used techniques for interface traps characterization rely on various combinations of capacitance-voltage and AC admittance-voltage / frequency measurements. These methods have been mostly developed nearly half a century ago and were tailored upon the case of the then overwhelmingly dominant Si/SiO_2 system [5].

However, experience indicates that blindly applying these techniques to high mobility semiconductor/ high-k stacks may lead to very inaccurate results [6]. Several complications need to be mentioned.

First, MOS devices fabricated on high-mobility semiconductors usually exhibit a much higher density of interface traps as compared to the Si/SiO_2 case [7]. An extreme D_{IT} might provide a trap-related capacitance component large enough to overcome the oxide capacitance ($C_{OX} < q\ D_{IT}$), delivering a dominant contribution to the measured impedance (see Fig. 2.4).

The second issue refers to the case of semiconductors with band gap significantly smaller than the silicon gap ($E_g(Si) = 1.12$ eV at 300K). Due to the high generation rate, the minority carriers become able to respond to the probing AC signal even at high frequencies. As a result, their contribution to capacitance and admittance signals overlaps with the features associated with interface traps, precluding any reliable analysis.

Furthermore, it has been repeteadly observed that a significant portion of the trap densities lies close to the semiconductor band gap edges. As a result, it appears difficult to reach the high-frequency regime in the capacitance measurements which, in turn, makes it difficult to determine the flat-band voltage (V_{FB}) point on the CV curve.

Third, as mentioned in the beginning of this chapter, several authors have already reported on a significant contribution of traps to the AC conductance in the low-frequency range ($f < 100$ Hz) [4] [1] [8] [9]. This much larger time constant (> 10 ms) as compared to the "true" interfacial states ($\tau < 1$ ms), makes practically impossible quantitative analysis of these *slow* traps by using conventional room-temperature AC admittance measurements.

Also, the slow traps induce a hysteresis in the CV curves making it difficult to estimate the flat-band voltage V_{FB} even when the high-frequency

regime can be reached.

In the past, several alternative models for the admittance of a MOS structure have been advanced which would account for some of the issues mentioned above [10], [11] [12]. Nevertheless, interpretation of the admittance response of high-mobility semiconductor/high-k insulator interfaces is still under debate (for example, the minority carriers contribution is often ignored in the literature). On the other hand, feasible characterization methodologies based upon those models, albeit improved, often require full processing of a gate-controlled diode or a MOS transistor thus introducing uncertainty related to the processing-induced interface damage [6].

Recently, we have demonstrated [13] that a feasible solution to the above issues can be found through the re-introduction of the Saturation suface PhotoVoltage (SPV) technique. In particular, it was shown how the determination of the semiconductor surface potential by means of SPV measurements allows one to accurately evaluate the D_{IT} in a simple MOS capacitor structure.

Moreover, this SPV methodology overcomes several practical limitations of the CV and GV-based characterization techniques. For example, whereas a low level leakage currents are often able to affect the conductance data, thus hindering D_{IT} extraction, they would influence SPV results marginally. Another complication might arise due to a large series resistance to the sample, leading to a large frequency dispersion of the CV and GV characteristics. This issue is particularly relevant for high-mobility semiconductor channel materials, largely produced as multilayered stacks containing buried junction regions. As mentioned in Chapter 2, the verification and assesment of the SPV experimental implementation has been done by performing a series of control measurements, which are summarized in the Appendix A.

5.2 Interface trap characterization in Ge/Sc-doped GeO_2/HfO_2 structures by SPV and AC conductance measurements

In this section, we describe CV, AC conductance and SPV measurements performed on a set of Ge/HfO_2 capacitors fabricated on single-crystal Ge wafers and passivated by different combinations of GeO_2 and Sc_2O_3 insulators. Interface trap densities and energy distributions determined on the basis of these measurements are compared, revealing dominant role of slow, oxide-related traps.

5.2.1 Description of the samples

Starting from an HF (2%) dip for 30 seconds of the (100) Ge wafers, the passivating Sc_2O_3 layers were grown by ALD process at 300 $^\circ C$, whereas GeO_2 layers were produced by plasma O_2 oxidation (plasma conditions 400 W, 5 sec, 300 $^\circ C$).

Pairs of n- and p-type Ge sample with different combinations of the two oxide passivating interlayers were compared: In samples 1 and 2 an intermixed oxide was used (0.5 nm Sc_2O_3 layer grown directly on the HF-last Ge wafer followed by the plasma oxidation); In samples 3 and 4 no oxidation was carried out and only 1.5 nm thick Sc_2O_3 film was deposited. Finally, all samples were capped with 10 nm HfO_2 insulating layer grown by ALD at 300 $^\circ C$ using $HfCl_4$ and H_2O as precursors. More details on the fabrication of the Sc_2O_3 layers can be found elsewhere [14]. MOS capacitors were completed by evaporation of semitransparent (15 nm thick) Au electrodes on top of the HfO_2. Backside contacts to Ge substrate were fabricated by evaporation of a thick Al contact layer (~ 0.5 μm thick).

5.2.2 Results

Fig. 5.1(a - d) shows the 100 Hz and 100 kHz CV curves as measured on the n-type samples 1 and 3 (Fig.5.1(a),(c)) and the p-type samples 2 and 4 (Fig.5.1(b),(d)). Fig.5.1(e),(f) compares the corresponding surface potential measured as a function of gate bias by using the SPV technique to the ideal curve computed according to Ref. [5] (blue curves). Comparison between the experimental and theoretical curves indicates that the surface potential can be efficiently swept across the entire Ge band gap. However, less steep variation of the experimentally measured ψ_S versus gate voltage V_G signals the influence of interface traps.

A first noteworthy consideration concerns the estimation of the flat-band voltage V_{FB}. Whereas it is known that both interface traps and minority carriers generation / recombination complicate the V_{FB} extraction from CV curves, this is rather straighforward from SPV measurements: The zero-crossing of the SPV curves reported in Fig. 5.1(e) and (f) can be reliably found at $V_{FB} \approx 0.25 \pm 0.05$ V for the n-type samples and $V_{FB} \approx -0.1 \pm 0.1$ V for the p-type samples.

A second point regards the defect densities. The large hysteresis affecting the CV curves also reveals the presence of a high density of slow charge trapping centers which, as previously mentioned, would require unfeasibly low test frequencies to be characterized. As an example, Fig. 5.2 shows the AC conductance peaks as measured in samples 3 and 4. The most pronounced

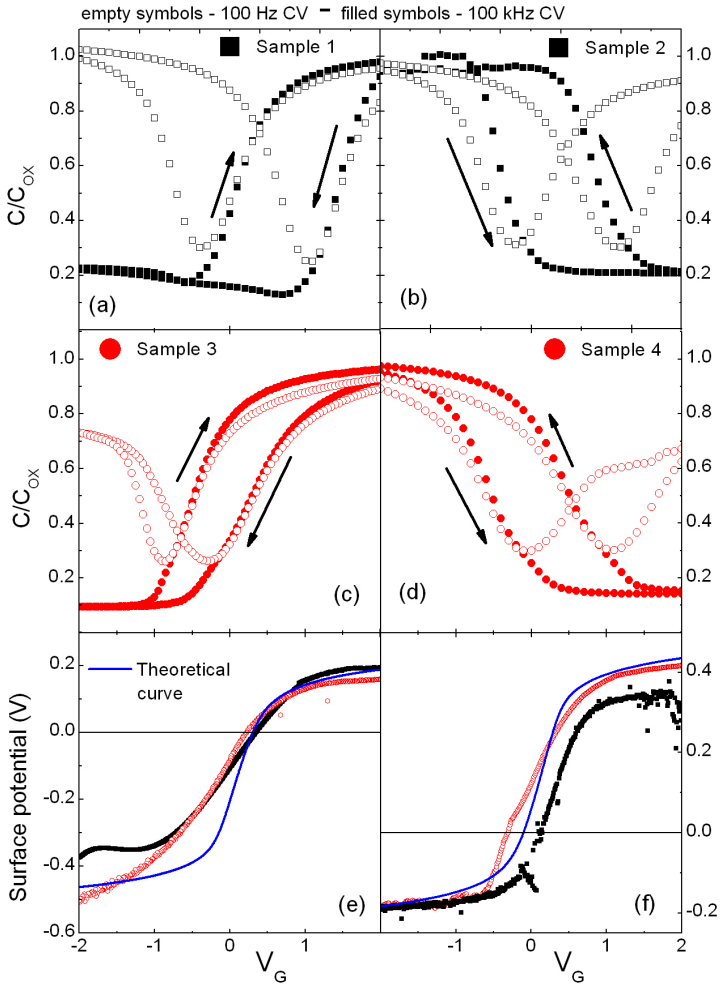


Figure 5.1: (a),(b),(c),(d) CV curves as measured on n-type samples 1 and 3 [(a) and (c)] and on the p-type samples 2 and 4 [(b) and (d)] at room temperature at 100 Hz and 100 kHz (empty and filled symbols, respectively). (e),(f) Surface potential versus gate bias curves as measured by mean of SPV on samples n-type samples 1 and 3 (e) and p-type samples 2 and 4 (f). On both plots the theoretical curve is also reported (blue curve).

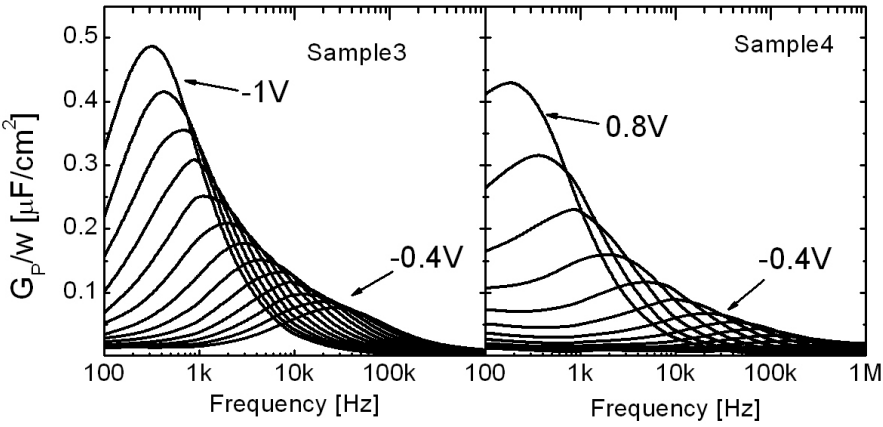


Figure 5.2: AC conductance (G_P/ω parallel conductance, angular frequency ratio) as a function of the AC signal frequency as measured on samples 3 and 4 as measured at room temperature. The gate bias V_G is indicated as the parameter and is varied in 0.05 V steps (sample 3) or 0.1 V steps (sample 4).

conductance peaks correspond to the highest D_{IT} values, are observed at low frequencies ($\approx$ 100 Hz).

At the same time, the low frequency CV curves shown in Fig.5.1(a - d), reveal the capacitance increase in inversion, indicative of minority carriers generation response (see, e.g., page 105 of Ref.[5]). This delivers additional conductance response (see Ref. [7]) making extraction of D_{IT} from the AC conductance measurements unreliable.

The D_{IT} energy distributions inferred from the AC conductance and SPV methods on all studied samples are compared in Fig. 5.3. The defect energy distributions extracted from the AC conductance method (open symbols) are U-shaped and closely resemble the interface trap energy profiles previously observed at the Ge/HfO_2 interface [2] [4].

The defect densities inferred by the AC conductance method lie in the range of 0.8 to $2 \cdot 10^{12} cm^{-2} eV^{-1}$ in the mid gap region, while the large hysteresis of the CV curves suggests the total trap density to be much higher. At the same time, the D_{IT} distributions obtained by the SPV method (filled symbols) reveal a more uniform distribution with typical densities of 5 to $10 \cdot 10^{12} cm^{-2} eV^{-1}$ at around mid gap in all the analyzed samples. This density can be compared to the density of oxide traps calculated from the 2 V hysteresis on the CV curves. This hysteresis correspond to a defect density of about $1.1 \cdot 10^{13} cm^{-2}$ (indicated as a dashed line in Fig. 5.3) assuming most of the traps to be located close to

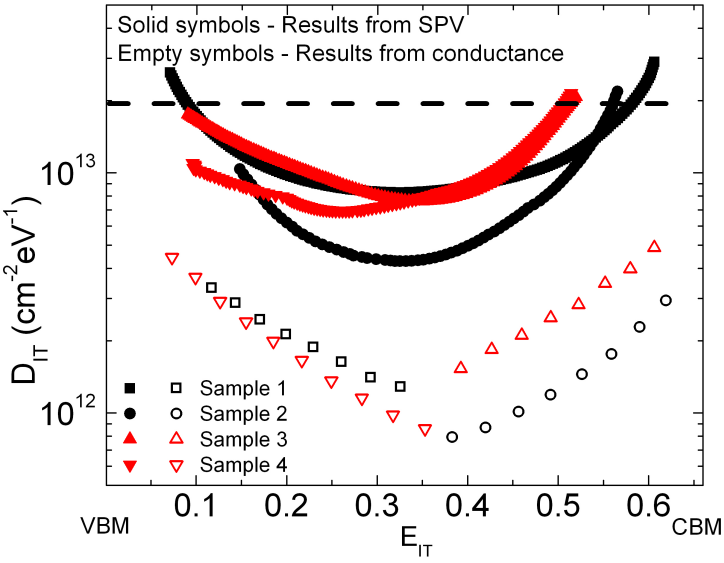


Figure 5.3: D_{IT} distributions as estimated through the AC-conductance method (empty symbols) and SPV technique (filled symbols) on all. The dashed line indicates the trap density required to give rise to a CV curve hysteresis of about 2 V.

the surface of Ge.

From this comparison one may conclude thet the majority of the charge trapping occurs on centers characterized by a large time constant (> 10 ms), giving rise to the large hysteresis of the CV curves. However, the large time constant makes them largely "invisible" to the conventional room temperature AC conductance method, which senses only fast interface states and, therefore, gives apparently lower D_{IT}.

5.3 Defect densities at Ge/high-k interfaces studied by the SPV method

As shown in the previous section, results obtained by means of SPV spectroscopy appear to be more representative for the real D_{IT} values at Ge/oxide interfaces. In this section we apply this method to analyze Ge-based devices with different interface passivation layers.

5.3.1 Description of samples

Two sets of samples have been additionally studied: The first set comprises 3 samples with a thick ($> 1\mu m$) epitaxially grown Ge film on Si (Ge *virtual substrate*, V.S.) and a multilayered insulator (Ge oxide, alumina and hafnia). After a 2 % HF deep for 30 sec, 4 or 1 nm Al_2O_3 were deposited by using ALD at 300 K with TMA and H_2O as precursors. Then, O_2 plasma oxidation of Ge was performed through the alumina layer (10 sec at 300 K). This process was intended to form a thin Ge oxide IL. Whereas one sample was kept with only the Ge oxide interlayer and a 4 nm thick Al_2O_3, on the other samples $\approx$ 2 nm HfO_2 was deposited by ALD (40 cycles, $HfCl_2/H_2O$ precursors). Successive XPS experiments were performed to evaluate the final thicknesses of the insulating layers yielding results reported in Table 5.1.

Table 5.1: Composition and thickness of the oxide insulator stack deposited on the Si/Ge V.S. samples.

HfO_2 (nm)	Al_2O_3 (nm)	GeO_X (nm)
-	3.9	0.82
2.26	0.59	1.04
2.49	0.77	0

The second set of samples was also fabricated on a thick ($> 2\mu m$) Ge buffer on a Si carrier wafer. Whereas one sample was kept as reference, on the other 2 samples strained SiGeSn alloys were grown by Reduced Pressure Chemical Vapor Deposition (RPCVD) using $SnCl_4$ and Si_2H_6 as precursors. The final thickness and Si and Sn concentrations were determined by RBS and are reported in Table 5.2. After a HF:HCl-last surface cleaning, 10 nm HfO_2 films were deposited on all samples by ALD using tetrakismetylamino hafium and ozone at 300 °C. More details on this fabrication process can be found in the literature [15].

Table 5.2: Composition and thickness of the Si/Ge V.S./$Si_XGe_YSn_Z$/HfO_2 samples.

Substrate	Channel	Oxide
Ge V.S. ($> 2\mu m$)	-	10 nm HfO_2
Ge V.S. ($> 2\mu m$)	93 nm $Si_{14\ \%}GeSn_{5\ \%}$	10 nm HfO_2
Ge V.S. ($> 2\mu m$)	437 nm $GeSn_{12.5\ \%}$	10 nm HfO_2

5.3.2 Results

Fig. 5.4 compares the D_{IT} energy distributions extracted on the Ge/Sc-doped GeO_X/HfO_2 samples discussed in the previous section to the ones obtained

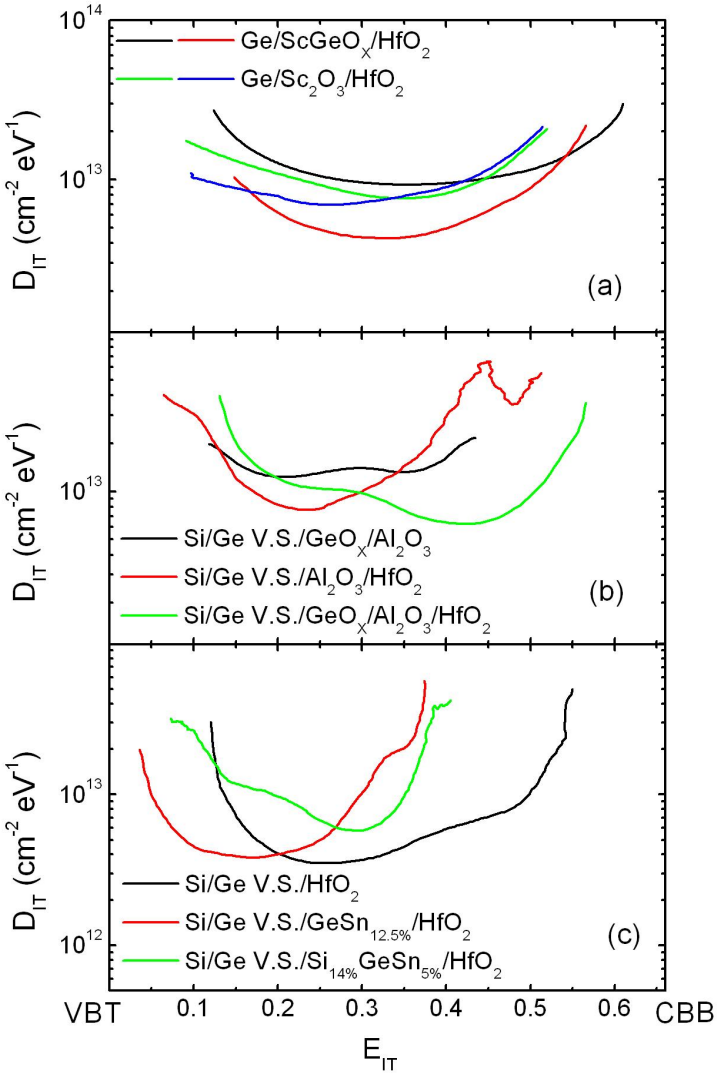


Figure 5.4: D_{IT} energy distributions as extracted through the SPV technique on a set of samples including the previously studied Ge/Sc-doped GeO_X/HfO_2 samples (a), samples fabricated on a Ge *virtual substrate* passivated by a GeO_X interlayer and a multi-layered Al_2O_3 and HfO_2 insulator (b), and samples provided with a $Si_XGe_ySn_Z$ channel layer and HfO_2 insulator (c).

on the Ge V.S. samples with the multilayer GeO_X - Al_2O_3 and HfO_2 insulators, and the samples fabricated on the $Si_XGe_YSn_Z$ layers of different compositions, grown on a Ge V.S. and HfO_2 insulator (Black, blue and red bold curves, respectively).

Importantly, whereas the whole figure is referenced to the bandgap of pure Ge, the $Si_XGe_YSn_Z$ samples have different widths for the semiconductor bandgap. In order to mantain a fair comparison from the view-point of the D_{IT}, the trap distributions as extracted on the SiGeSn samples (red bold curves) have been aligned to the VBM of Ge because internal photoemission experiments (not discussed here) indicate that the energy of the VBT in the $Si_XGe_YSn_Z$ alloys in the studied range of composition remains the same as in pure Ge.

This comparison of the D_{IT} energy distributions reveals several interesting features. As it can be seen, on average, they are universally characterized by a U-shaped distribution with an average trap density of around $9 \pm 3 \cdot 10^{12} cm^{-2} eV^{-1}$. This result is remarkable by considering that standard H_2-passivation of the Si/SiO_2 interfaces allows one to achieve D_{IT} below $10^{11} cm^{-2} eV^{-1}$.

Similarity of the results obtained on samples fabricated using different passivation schemes and the earlier discussed high density of slow traps, provides a clear indication that the dominant contribution to this high D_{IT}s imparing electrical quality of the Ge/oxide interfaces originates from the traps in the oxide stack. At the same time, since similar high-k insulators deposited on the control Si wafers result in significantly lower D_{IT} (see, as an example, Fig. 4 in Ref. [16]), one must come to the conclusion that the presence of Ge at the interface has significant influence on the oxide trapping. Therefore, in order to shed some light on the mechanism of this influence in the next chapter we will specifically address the Ge-related traps in HfO_2.

5.4 Conclusions

In this chapter, we have shown that the Saturation surface PhotoVoltage technique is suitable for the quantification of interface traps in high-mobility / high-k MOS capacitors. Its effectiveness has been assessed by a comparative study, including CV and AC conductance measurements, on a case study of Ge/HfO_2 samples passivated by different combinations of Sc_2O_3 and GeO_2. Enhanced generation of minority carriers at room temperature, a major feature of narrow band gap materials, does not affect SPV results. At the same time, by monitoring the (quasi)-static band bending in the semiconductor one can reveal the presence of traps with a large time constant. These slow traps, commonly associated with defects in the oxide layer, can be probed even at room temperature.

We have then extended in the SPV study to a larger set of interfaces between Ge-based semiconductors and HfO_2 with different passivation shemes.

The results have suggest the existence of a common cotribution to the interface trap density of slow traps stemming from the oxide defects. The origin of the latter will be further explored in the next chapter.

Bibliography

[1] V.V. Afanas'ev, Y.G. Fedorenko, and A. Stesmans *Interface traps and dangling-bond defects in (100)Ge/HfO_2* Appl. Phys. Lett., **87**(3), 032107 (2005)

[2] V.V. Afanas'ev and A. Stesmans *Spectroscopy of electron states of interfaces of (100)Ge with high-k insulators* J. Mat. Sci. Semicon. Proc., **9**, 764 (2006)

[3] A. Toriumi, T. Tabata, C. Lee, T. Nishimura, K. Kita, and K. Nagashio *Opportunities and challenges for Ge CMOS - Control of interfacing field on Ge is a key* Microelectron. Eng., **86**, 1571 (2009)

[4] N. Taoka, W. Mizubayashi, Y. Morita, S. Migita, H. Ota, and S. Takagi, *Nature of interface traps in Ge metal-insulator-semiconductor structures with GeO_2 interfacial layers* J. Appl. Phys., **109**(8), 084508 (2011)

[5] E.H. Nicollian, and J.R. Brews *MOS(Metal Oxide Semiconductor) Physics and technology* (Wiley-Interscience, NewYork, 1982)

[6] K. Martens, C.O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, E. Maes, and G. Groeseneken *On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates* IEEE Trans. Electron Dev., **55**(2), 547 (2008)

[7] R. Engel-Herbert, Y. Hwang, and S. Stemmer *Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces* J. Appl. Phys., **108**, 124101 (2010)

[8] C.L. Hinkle, M. Milojevic, B. Brennan, A.M. Sonnet, F.S. Aguirre-Tostado, G.J. Hughes, E.M. Vogel, and R.M. Wallace *Detection of Ga suboxides and their impact on III-V passivation and Fermi-level pinning* Appl. Phys. Lett., **94**, 162101 (2009)

[9] E. J. Kim, L. Wang, P.M. Asbeck, K.C. Saraswat, and P. C. McIntyre *Border traps in $Al_2O_3/In_{0.53}Ga_{0.47}As(100)$ gate stacks and their passivation by hydrogen anneals* Appl. Phys. Lett., **96**, 012906 (2010)

[10] T.E. Kazior, J. Lagowski, and H.C. Gatos *The electrical behavior of GaAs/insulator interfaces: A discrete energy interface state model* J. Appl. Phys., **54**, 2533 (1983)

[11] K. Martens, W. Wang, K. De Keersmaecker, G. Borghs, G. Groeseneken, and H. Maes *Impact of weak Fermi-level pinning on the correct interpretation of III-V MOS C-V and G-V characteristics* Microelectron. Eng., **84**, 2146 (2007)

[12] X. Sun, C. Merckling, G. Brammertz, D. Lin, J. Dekoster, S. Cui, and T.P. Ma *Improved AC conductance and Gray-Brown methods to characterize fast and slow traps in Ge metal-oxide-semiconductor capacitors* J. Appl. Phys., **111**(5), 054102 (2012)

[13] O. Madia, V. Afanas'ev, D. Cott, H. Arimura, C. Schulte-Braucks, H.C. Lin, D. Buca, N. Von Den Driesch, L. Nyns, T. Ivanov, D. Cuypers, and A. Stesmans *Saturation Photo-Voltage Methodology for Semiconductor/Insulator Interface Trap Spectroscopy* ECS J. Solid State Sci. Tech., **5**(4), 3031 (2016)

[14] L. Nyns, J.G. Lisoni, G. Van den Bosch, S. Van Elshocht, and J. Van Houdt, *Atomic layer deposition of scandium-based oxides* Phys. Status Solidi A, **211**(2), 409 (2014)

[15] S, Wirths, R. Geiger, N. Von Den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chiussi, J. Hartmann, H. Sigg, J. Faist, D. Buca, and D. Grützmacher *Lasing in direct-bandgap GeSn alloy grown on Si* Nature Photonics, **9**(2), 88 (2015)

[16] Y.G. Fedorenko, L. Truong, V. Afanas'ev, and A. Stesmans *Interface state energy distribution in (100)Si/HfO_2* Mat. Sci. Semicond. Proc., **7**(4), 185 (2004)

Chapter 6

Intrinsic and Ge-related deep electron traps in ALD-grown HfO_2

The interface trap density data presented in the previous chapter suggest that the majority of charge trapping centers at Ge/oxide interface are *slow* oxide-related traps. Importantly, very similar D_{IT} distributions are found in samples with different passivation layers, indicating a common component of the trap spectrum is related to the presence of Ge.

In the previous studies of Toriumi *et. al.* and Taoka *et. al.*, the growth of a GeO_2 interlayer is shown to provide a reasonably good passivation of Ge interfaces with high-k insulating oxides [1][2]. Processing in a O-rich environment blocks the desorption of GeO (Ge monoxide) species, which are inevitably formed at the interface between Ge and the oxide insulators at elevated temperatures.

Yet, this explanation still leaves some key observations unexplained. Specifically, enhanced electron trapping is also found in $SiGe/HfO_2$ entities annealed at a high temperature ($> 1000\ ^{\circ}C$), at which Ge oxide becomes unstable (samples as fabricated in Ref. [3]). Furthermore, the threshold voltage instability ascribed to electron trapping (positive bias temperature instability, PBTI) is more pronounced in Ge MOS devices than in Si reference counterparts with the same high-k insulator. It then appears that increased charge trapping correlates with the presence of Ge in the oxide.

As mentioned in Chapter 4, the high diffusivity of Ge upon thermal process is well known. Therefore, it is reasonable to address the effect of Ge out-diffusion on the trapping properties of high-k oxides. Ge-related electron

traps are known in SiO_2 [4], while Ge impurities are theoretically predicted to give rise to deep gap states in HfO_2 and other high-k insulators [5][6].

For these reasons, in this chapter the Exhaustive PhotoDepopulation Spectroscopy is applied to a set of samples with Ge-doped HfO_2 layers. This technique allows one to study the energy depth distribution of the oxide traps. Comparison of the results obtained in the control (Ge-free) and Ge-doped HfO_2 layers reveals how the presence of Ge correlates with additional electron traps in the insulator. The resolved spectral distribution of the newly revealed traps is found to lie at about ≈ 3 eV below the CBB of HfO_2, in overlap with the band gap of Ge. Furthermore, it is found that no significant contribution to the traps density arises from donor states. The dominance of acceptor states agrees with the earlier mentioned enhanced electron trapping in Ge MOS devices.

6.1 Sample preparation

Considering the mentioned enhanced charge instability in Ge interfaces, the present experiments required the fabrication of dedicated samples so that charge trapping effects in the oxide can be reliably isolated from the interface trapping. As a result, the studied samples were prepared on n-type (100) Si substrates with a thermally grown 5-nm thick SiO_2 layer to serve as a *tunnel* oxide and ensuring low density of interface traps. Next, 1- or 2- monolayer (ML) thick Ge films were sputtered on top of the SiO_2 and subsequently capped by 20 nm of ALD-grown HfO_2. The control sample was Ge-free and served as reference revealing the intrinsic traps in HfO_2.

In the following discussion a code is used to refer to the three types of samples: S0 (no Ge), S1 (1 ML of Ge), and S2 (2 ML of Ge). Deposition of hafnia was performed using atomic layer deposition (ALD) from a chlorine-free precursor to attain a lower density of HfO_2-related traps, as compared to films grown using $HfCl_4$ [7].

Electron traps in the SiO_2/HfO_2 insulating stacks were studied both in the as-deposited state and after 30 min annealing in N_2 at 500 $^\circ C$, 700 $^\circ C$ or 1000 $^\circ C$ to reveal the impact of Ge diffusion into the HfO_2 film. Upon each annealing step, the samples were treated for 15 min in H_2 (1.1 atm, 400 $^\circ C$) to passivate Si/SiO_2 interface states. MOS capacitors were prepared by evaporation of semitransparent (13 nm) Au electrodes on top of the oxide stack. The schematic cross section of the samples is shown in Fig. 6.1

6.2 Results

The light-induced oxide charge variations as a function of photon energy $\delta Q(h\upsilon)$ as measured on the un-annealed samples S0, S1 and S2 before and

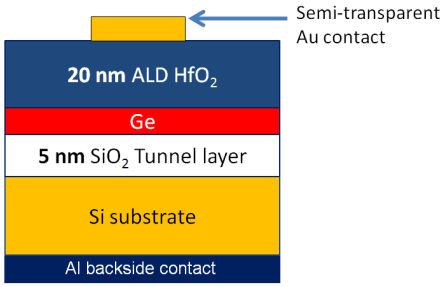


Figure 6.1: Schematic representation of the fabricated samples. Sample S0 was kept Ge-free and used as the reference. On samples S1 and S2 respectively 1ML and 2ML of Ge were sputtered on top of the SiO_2 tunnel layer.

after electron injection (black and red curves, respectively) are shown in Fig. 6.2(a - c). For this experiment electron injection was induced by applying a +17 V voltage pulse to the Au electrode since this charging pulse amplitude corresponds to saturation of the oxide trapped charge.

As explained more in detail in chapter 2, depending on the photon energy range, the oxide charging reflects three different processes. First, for low photon energies ($h\upsilon < 4.25$ eV, which value is indicated by a vertical dashed line in Fig. 6.2), the charge changes due ionization of gap states. Second, for higher photon energies ($h\upsilon > 4.25$ eV), trapping of electrons injected by internal photoemission (IPE) from the Si substrate over the SiO_2 tunneling barrier occurs. Finally, when the photon energy exceeds the bandgap width of HfO_2 (5.6 eV), generation of $e^- - h^+$ pairs in the oxide (PhotoConductivity, PC) leads to accumulation of positive charge due to holes drifting towards the Si/SiO_2 substrate [8].

From Fig. 6.2 it can be noticed that only a limited (positive) charging is found in all the pristine HfO_2 films (black curves in Fig. 6.2(a),(b),(c)). The picture is changed after electron injection, which results in trapping of a net negative charge (-0.9 to -1 μCcm^{-2}) in all analyzed samples.

These results indicate that the majority of charge trapping centers in HfO_2 films are of acceptor nature [electron-traps, corresponding to the (0/-) charge transition]. Also, one can notice that the weak photo-induced positive charging in pristine samples occurs in the same spectral range as the de-populated acceptor states, suggesting that a (small) fraction of the acceptors is populated by electrons during sample processing. Additionally, the measurable positive charging can only be observed for photon energies larger than 5.5 eV, i.e., above the HfO_2 PC onset. These results indicate that the density of donor states contributing to charging by a (0/+) transition with energy levels inside

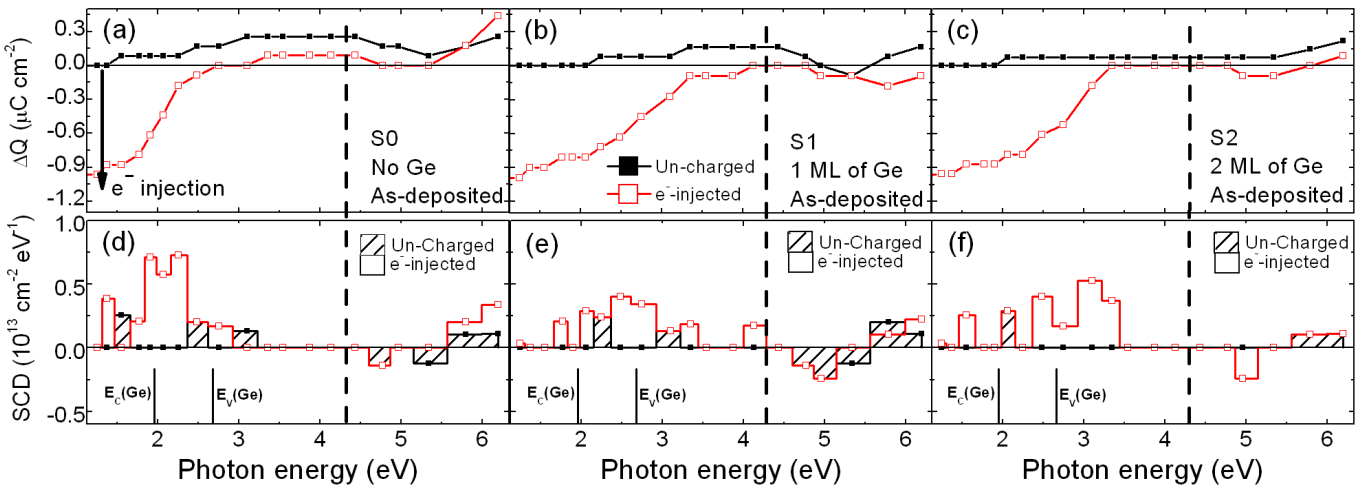


Figure 6.2: Illumination-induced charge variation (a-c) and Spectral Charge Density distributions (d-f) versus photon energy, as measured in as-received $Si/SiO_2/HfO_2/Au$ structures without Ge contamination (a),(d) and in samples containing 1ML (b),(e) and 2 MLs (c),(f) of Ge between the SiO_2 tunneling layer and the HfO_2 film. Dashed lines indicate the energy onset of electron IPE from the Si substrate. The energy position of the Ge bandgap edges are indicated in panels (d),(e) and (f). Origin of the energy scale corresponds to the HfO_2 CBB.

the HfO_2 band gap is below detection limit ($\approx 5 \times 10^{11} cm^{-2}$).

The latter observation is consistent with the earlier reported charge injection experiments on ALD-grown oxides (Al_2O_3, ZrO_2, HfO_2) where no measurable hole trapping was found [8]. Further affirming this inference, no sign of donor states was reported in HfO_2 films deposited on Si substrate [7][9]. Taking into account that deep donor states are expected to be related to O-vacancies in HfO_2 [10][11], these experimental results suggest that these defects are not present in the ALD-grown HfO_2 in any substantial concentration. Nonetheless, recently [12] a new oxygen vacancy defect configuration was proposed, which would be able to trap negative charges.

Fig. 6.2(a),(b),(c) also shows that the trapped electrons can be completely removed from the oxide by sustained illumination, indicating that EPDS results reflect the energy distribution of the vast majority of electron traps. Remarkably, whereas in the Ge-free sample S0 most of the trapped electrons are released (the injected negative charge is removed) by photons with $h\nu < 2.5$ eV, depopulation of electron traps in the Ge-containing samples S1 and S2 requires higher photon energies and complete depopulation occurs only in the spectral range 2.5 - 3.5 eV. This difference suggests that the presence of Ge in the oxide insulator generates deep electron traps.

The same behavior can be seen in panels (d-f) of Fig. 6.2, comparing the infered SCD energy distributions. Since these distributions correspond to removal of an electron from a gap state into the oxide CB, the zero on the energy scale of the shown SCD distributions corresponds to the HfO_2 CBB.

The red open bars in these graphs show the SCD observed after electron injection from the silicon substrate. As can be seen, the Ge-free sample S0 (Fig. 6.2(d)) exhibits an SCD peak energetically centered at around ≈ 2 eV below the HfO_2 CB, while the SCD spectra of samples S1 and S2 reveal broader and deeper trap distributions in the energy interval 2.5 - 3.5 eV below the HfO_2 CB. This suggests that Ge atoms incorporated into the oxide network give rise to deep acceptor states (electron traps). Furthermore, the energy distribution of these traps overlaps with the Ge band gap energy interval, as in dicated in Fig. 6.2(d),(e),(f). Therefore, these oxide traps will electrically behave as slow interface traps once electron tunneling from Ge becomes possible.

As mentioned before, the same level of electron trap filling was achieved in all analyzed samples by applying a voltage pulse of +17 or +20 V in amplitude.

The results shown in Fig. 6.2 suggest that in the Ge-doped HfO_2 contribution of "shallow" intrinsic traps becomes insignificant. Nevertheless, the shallow acceptors are still present in the oxide as revealed by the SCD distributions evaluated for different filling pulse amplitudes, and shown in Fig. 6.3. A color map, from cold (black) to warm (red) colors is used to show the SCD evolution with increasing pulse amplitude.

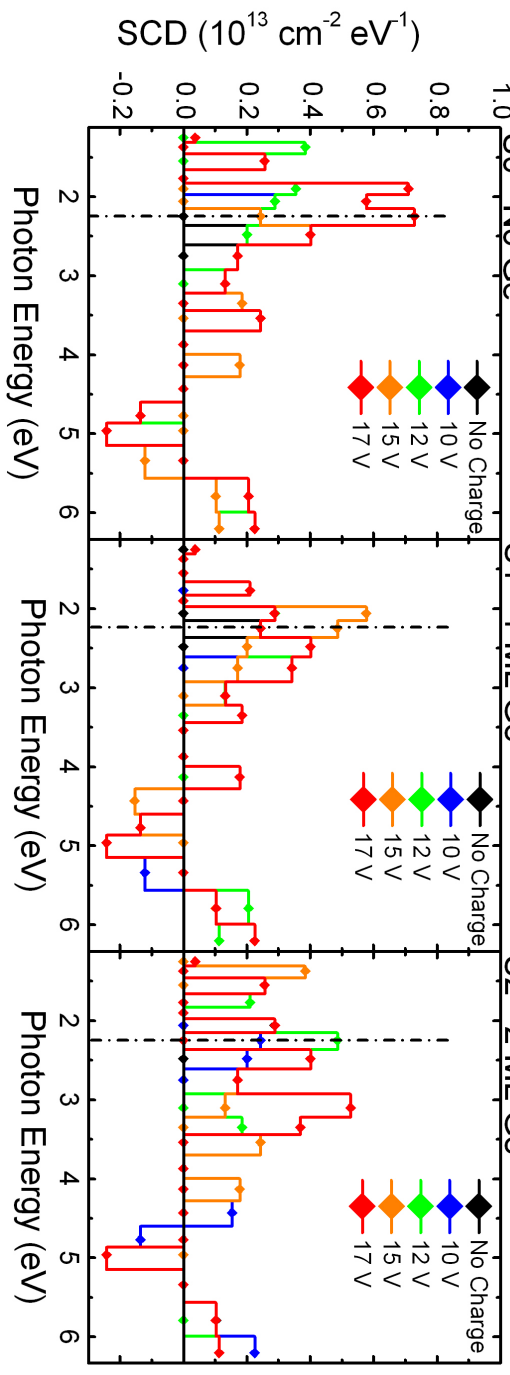


Figure 6.3: Spectral Charge Density distributions versus photon energy, as measured on as-received samples S0, S1 and S2 subject to different levels of electron injection. A color scale (cold to warm colors) is intended to highlight how deeper electron traps are constituted by a larger cross section, for they need larger voltage pulses to populate.

Apparently, the deep traps introduced by Ge impurity have larger electron capture cross section than the shallow "intrinsic" traps. With further increase of the filling pulse amplitude, the shallow traps become less pronounced as compared to deeper ones. This suggests field-induced de-population of the shallow acceptors.

Next, we addressed the effect of annealing on traps in samples S0 (no Ge) and S2 (2 MLs of Ge), to evaluate the effect of Ge diffusion. Previous studies [13] of HfO_2 deposited on Ge substrates indicate Ge in-diffusion and incorporation into the oxide do occur upon thermal treatment in N_2 at $T_{annealing} > 600\ ^\circ C$. Therefore, we analyzed the electron trap distribution in samples annealed at 500, 700 or 1000 $^\circ C$ in N_2. For each sample, two cycles of electron injection, at +17 V and +20 V, have been performed to ensure reproducibility of the results.

Fig. 6.4(a,b) compares the SCD distributions in samples S0 and S2 annealed at 500 $^\circ C$. This annealing step drastically affects the densities of shallow and deep intrinsic traps, as compared to the as-deposited HfO_2 (Fig. 6.2 and 6.3): The density of shallow acceptors ($E_t \approx 2$ eV) significantly decreases in sample S0 (no Ge), while the density of deeper traps ($E_t \approx 3$ eV) becomes significantly higher. At the same time, the density of deep Ge-related traps is barely affected by the 500 $^\circ C$ anneal.

The trend of generating deep traps is further affirmed by the SCD distributions in samples S0 and S2 subject to annealing at 700 $^\circ C$ shown in Fig. 6.4(c),(d). While the density of acceptors distributed in the energy range 1.5 - 2.5 eV below the HfO_2 CBB does not change significantly, in the energy window between 2.5 to 4 eV the trap density increases. Whereas the trap spectra obtained for sample S0 in this range increases moderately from about 0.6 $\times 10^{13}$ to 0.9 $\times 10^{13} cm^{-2} eV - 1$, the trap spectral density in sample S2 is much higher, reaching 1.5 $\times 10^{13} cm^{-2} eV^{-1}$. The latter value approximately corresponds to the combined spectral density of deep intrinsic traps encountered in sample S0 and the Ge-related traps in the same energy window ($\approx 6 \times 10^{12} cm^{-2} eV^{-1}$ found in sample S2 upon anneal at lower temperature (Fig. 6.4(b)).

A remarkable feature of the trapped electrons energy distributions shown in Fig. 6.2 - 6.4 is their ≈ 1 eV energy width. However, before discussing this observation, one should exclude that the broadening of the energy spectrum represents a measurement artifact, i.e., incomplete removal of electrons at each illumination step. As mentioned in Chapter 2, we were able to guarantee the release of above 90 % of the charges present in the insulating film by illuminating the sample for 45 min per spectral step $\Delta h\nu$. In order to confirm this, we repeated the EPDS measurements on samples S0 and S2 annealed at 700 $^\circ C$ with an increased illumination time (3 h per step instead of 45 min). The results, shown in Fig. 6.5(a),(b), demonstrate good agreement between the two distributions. Therefore, we can conclude that the shown

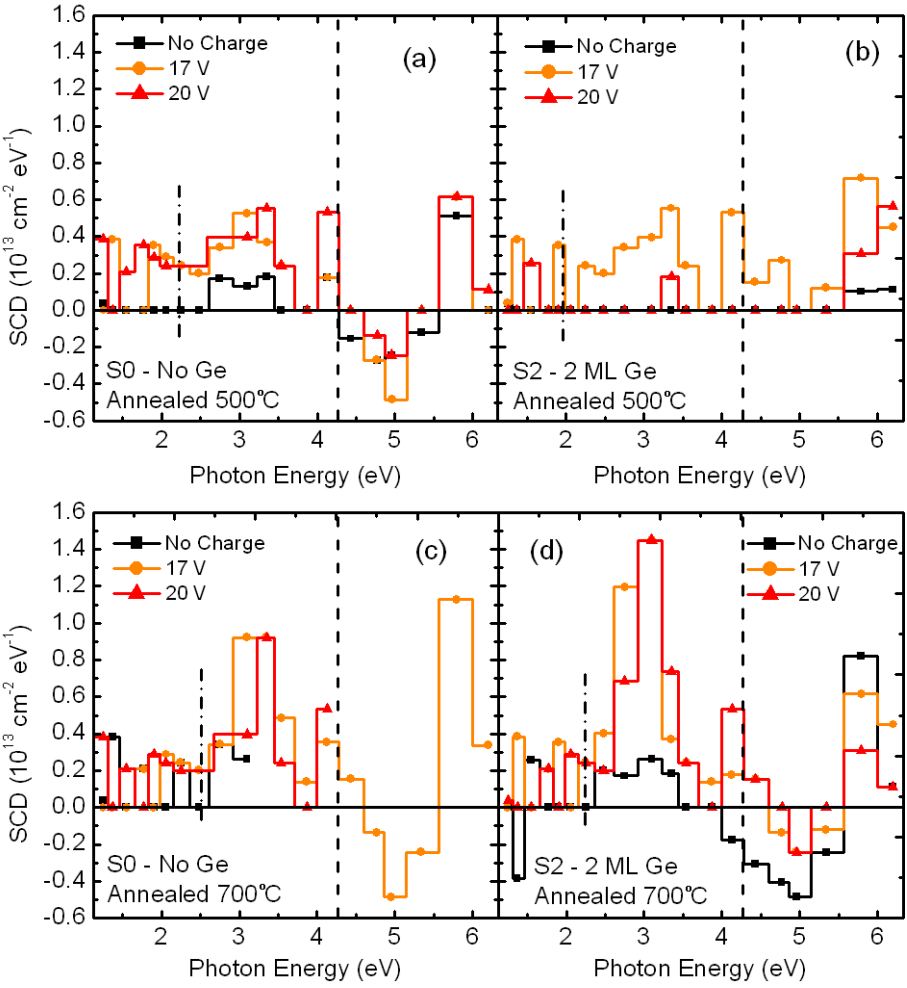


Figure 6.4: Spectral Charge Density distributions versus photon energy as measured in $Si/SiO_2/HfO_2/Au$ structures (sample S0) and $Si/SiO_2/2$ MLs $Ge/HfO_2/Au$ structures (sample S2) after post-deposition anneal in N_2 at 500 $°C$ (a),(b) and 700 $°C$ (c),(d). Results are reported for the pristine state (black bars) and for two electron injection levels (at +17 V and +20 V amplitude of the charge voltage pulse, orange and red bars, respectively). Dashed lines indicate the onset of electron IPE from the Si substrate. The dashed-dot lines intend to help the reader in distiguish two spectral regions behaving differently after the thermal treatments.

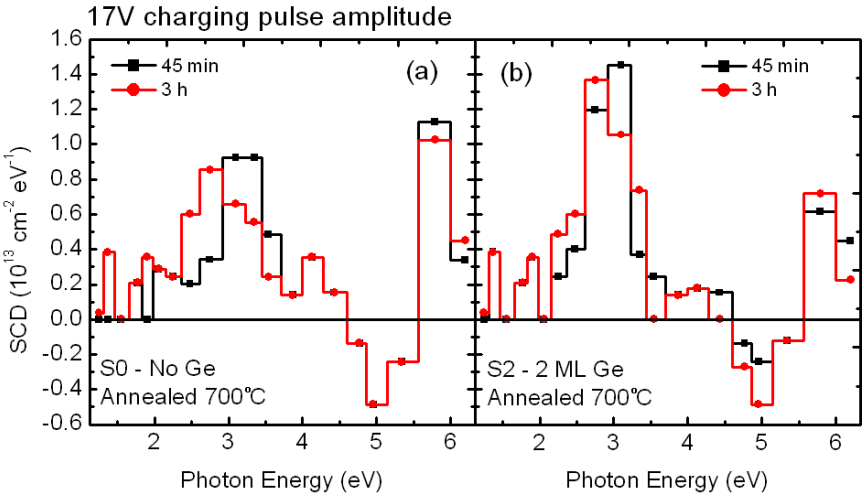


Figure 6.5: Spectral Charge Density distributions versus photon energy as measured in samples S0 and S2 after post-deposition anneal in N_2 at 700 $°C$ with +17 V amplitude of the charging voltage pulse. Red and black bars correspond to experiments performed with 45 min and 3 h illumination intervals.

spectral distributions are not artefacts of the experimental procedure and reflect considerable site-to-site variation of the trapped electron energy.

As reported by Zhang *et al.* [13], substantial incorporation of Ge atoms in HfO_2 deposited on Ge substrate is observed after annealing at temperatures starting from $\approx$ 600 $°C$. It is thus fair to expect that Ge atoms become mobile at 700 $°C$ and diffuse into the insulator. This may explain the generation of additional deep acceptor states upon 700 $°C$ anneal as compared to the samples annealed at 500 $°C$ [cf. Fig. 6.4(b),(d)].

The results obtained after annealing of samples S0 and S2 at 1000 $°C$ in N_2 are shown in Fig. 6.6(a),(b). As can be seen, the trap densities in the energy range of 2.2 - 4 eV significantly decrease and become comparable in both samples.

Since at this temperature Ge oxides are unstable (this temperature is in fact above the melting point of Ge itself), this result probably reflects evaporation of Ge atoms from the surface of the insulator, leading to elimination of the Ge-related traps. This conclusion is supported by a previous study of Ge-implanted SiO_2 layers where removal of the Ge-related electron traps has been observed after annealing at 1000 $°C$ in N_2 [4].

Resuming, two main conclusions can be drawn from the results discussed

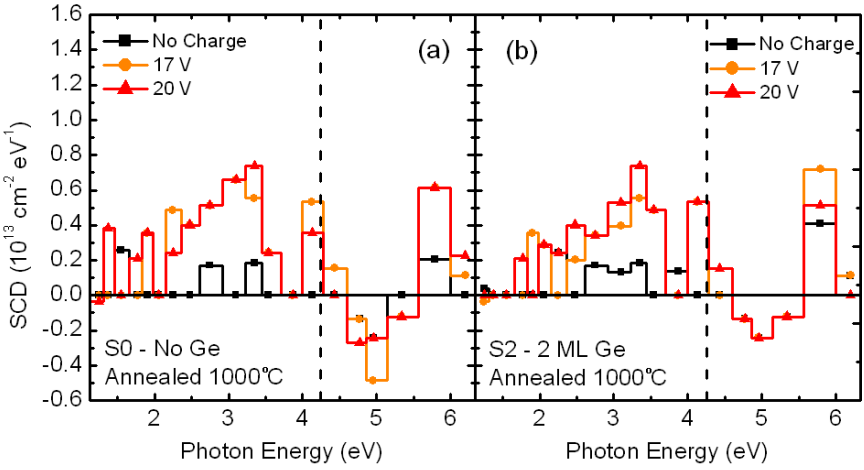


Figure 6.6: Spectral Charge Density distributions versus photon energy as measured in samples S0 (a) and S2 (b) after post-deposition anneal in N_2 at 1000 $°C$. Results are shown for the pristine sample (black bars) and for two electron injection levels induced by applying a voltage pulse of +17 V and +20 V amplitude (orange and red bars, respectively). Dashed lines indicate the onset of electron IPE from the Si substrate.

above. First, whereas no donor states (hole traps) are found to be present in the ALD-grown HfO_2 or in the Ge-doped HfO_2, large densities of acceptors states (electron traps) have been revealed.

Second, the results suggest correlation between the incorporation of Ge in HfO_2 films and generation of deep electron traps (acceptors) with a broad energy level distribution centered at about 3 eV below the CBB of the oxide insulator.

Fig. 6.7 shows the SCD distributions as probed in as-received samples S0 and S2 in combination with schematic band diagrams of the $Si/SiO_2/HfO_2$ entity. For comparison, Fig. 6.7 also shows the energy position of the band gap of Ge using band alignments experimentally determined by IPE [14]. This energy distribution of traps indicates that, besides explaining enhanced charge trapping in the oxide, the Ge-related defects may also contribute to interface trap densities since their energy distribution overlaps with the energy interval of the Ge bandgap at the interface with HfO_2.

This conclusion provides explanation to the high slow D_{IT} values discussed in Chapter 5. Noteworthy is that the SCD and the D_{IT} values

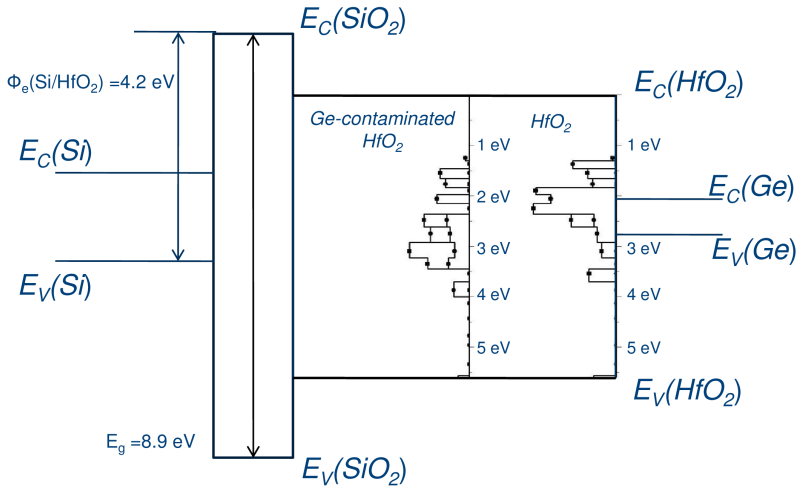


Figure 6.7: Band diagram of the un-annealed $Si/SiO_2/HfO_2$ structure with and without incorporation of Ge in the oxide. The Ge energy bandgap edges are indicated allowing comparison to the IPE data [14]

(about $\approx 10^{13} cm^{-2} eV^{-1}$, are in good agreement.

6.3 Conclusions

In this last chapter we have gained further insight in the origin of the high interface and oxide trap densities found at interfaces of Ge-based semiconductor materials with high-k insulators.

Supporting suggestions made in Chapter 5, it was found that a large contribution to the interface trap density in Ge-containing systems originates from defects within the oxide insulator. Moreover, SPV results obtained on samples fabricated with different high-k oxides and different passivations schemes indicate the existence of a common component related to the presence of Ge itself.

Using the EPDS methodology, we have found that while the ALD - grown HfO_2 contains a considerable density of shallow acceptor states (electron traps), incorporation of Ge atoms gives rise to deeper acceptors with a broad energy level distribution centered at around $\approx$ 3 eV below the HfO_2 CBB. These Ge-related defects contribute to interface trap densities since their energy distribution overlaps with the energy interval of the Ge bandgap at the interface

with HfO_2.

Bibliography

[1] A. Toriumi, T. Tabata, C. Hyun Lee, T. Nishimura, K. Kita, and K. Nagashio *Opportunities and challenges for Ge CMOS - Control of interfacing field on Ge is a key* Microelectron. Eng. **86**, 1571 (2009)

[2] N. Taoka, W. Mizubayashi, Y. Morita, S. Migita, H. Ota, and S. Takagi, *Nature of interface traps in Ge metal-insulator-semiconductor structures with GeO_2 interfacial layers* J. Appl. Phys. **109**(8), 084508 (2011)

[3] J. Franco, B. Kaczer, M. Toledano-Luque, P. J. Roussel, T. Kauerauf, J. Mitard, L. Witters, T. Grasser, and G. Groeseneken, *SiGe Channel Technology: Superior Reliability Toward Ultra-Thin EOT Devices - Part II: Time-Dependent Variability in Nanoscaled Devices and Other Reliability Issues* IEEE Trans. Electr. Devices, **60**(1), 405 (2013)

[4] J.M.M. de Nijs and P. Balk *Electron trapping properties of Ge-implanted SiO_2* Microelctron.Eng., **22**, 123 (1993)

[5] Q.Q. Sun, Y. Shi, L. Dong, H. Liu, S.-J. Ding, and D. W. Zhang, *Impact of germanium related defects on electrical performance of hafnium oxide* Appl. Phys. Lett., **92**(10), 102908 (2008)

[6] E. Golias, L. Tsetseris, A. Dimoulas, and S. T. Pantelides, *Ge volatilization products in high-k gate dielectrics* Microelectron. Eng., **88**(4), 427 (2011)

[7] V. V. Afanas'ev, W. C. Wang, F. Cerbu, O. Madia, M. Houssa, and A. Stesmans *Spectroscopy of Deep Gap States in High-k Insulators* ECS Trans., **64**(8), 17 (2014)

[8] V. V. Afanas'ev and A. Stesmans *Stable trapping of electrons and holes in deposited insulating oxides: Al_2O_3, ZrO_2, and HfO_2* J. Appl. Phys., **95**(5), 2518 (2004)

[9] W.C. Wang, M. Badylevich, C. Adelmann, J. Swerts, J.A. Kittl, and V. Afanasev *Electron trap energy distribution in ALD Al_2O_3, $LaAl_4O_X$, and $Gd_yAl_{2-y}O_3$ layers on Silicon* IOP Conf. Series: Mat. Sci. and Eng., **44**, 012008 (2012)

[10] S. J. Clark, L. Lin, and J. Robertson *On the identification of the oxygen vacancy in HfO_2* Microelectron. Eng., **88**, 1464 (2011)

[11] P. Broqvist and A. Pasquarello *Oxygen vacancy in monoclinic HfO_2: A consistent interpretation of trap assisted conduction, direct electron*

injection, and optical absorption experiments Appl. Phys. Lett., **89**(26), 262904 (2006)

[12] M. Watkins, and A. Shluger *Charge state switching of oxygen vacancies at HfO_2/SiO_2 interface* presented at INFOS 2015, Udine, Italy

[13] Q. Zhang, N. Wu, D. M. Y. Lai, Y. Nikolai, L. K. Bera, and C. Zhu *Germanium incorporation in HfO_2 dielectric on Germanium substrate semiconductor devices, materials, and processing* J. Electrochem. Soc., **153**, 207 (2006)

[14] V. V. Afanas'ev, *Electron Band Alignment at Interfaces of Semiconductors with Insulating Oxides: An Internal Photoemission Study* Adv. Condens. Matter. Phys., 301302 (2014)

Chapter 7

Conclusions and Outlook

7.1 Conclusions

At the moment this chapter is being laid down, the implementation of a Ge-based technology for the next generation of nanoelectronic devices seems to nearly come to reality. As already mentioned in the introduction, a test structure for the 7 nm technology node has recently been unveiled by a consortium involving IBM, Samsung and GlobalFoundries. This contains SiGe channel FinFETs, indicating that major players in the industry are moving into this direction. Also, Ge appears to be a material of choice for even more revolutionary concepts. For example, Ge has been recently used as the source for 2D TMD-based hole tunnel-FETs [1].

However, whereas the use of germanium in FET devices might guarantee further enhancement of performace, the electrically active defects will play a critical role in determining the success or failure of any specific design. In this PhD work we have sought to reveal the physical origin and dependences with respect to process parameters of defects present in several Ge-based technologies. While in Chapters 3 and 4 we addressed interfaces of SiGe, in Chapters 5 and 6 we focused on pure Ge devices. The total of this was intended to give a meaningful picture of some of the challenges that the microelectronic industry will face in the coming years: Implementation of pure Ge channels in FET devices will probably happen "gradually" through progressive alloying with Si.

In Chapter 3 we studied defects at the interfaces of $SiO_2/Si_{1-x}Ge_x/SiO_2$ heterostructures fabricated by the Ge-condesation technique. We found that the presence of residual strain in the $Si_{1-x}Ge_x$ layer has a dramatic impact on the density of interface defects -Ge P_{b1} dangling bond defect as established by ESR spectroscopy- as well as on their passivation efficiency by annealing in

H_2. As the strain is unavoidable in future technology nodes, this result implies that the Ge condensation growth, despite offering a number of advantages (i.e. possibility to fabricate high-Ge content SiGe layers over a large wafer area), might be largely unsuited for production use unless overgrowth of a less strained layer is implemented. More generally, our results suggest that the strain-based mobility boosting approach has natural limits related to defect formation.

In Chapter 4 we shifted our attention towards a more conventional process, where we investigated (100) Si/SiGe/Si/SiO_2/HfO_2 structures fabricated by epitaxial SiGe growth and provided with a state-of-the-art metal gate on top. By performing ESR experiments, we have revealed the presence of Si P_{b0} dangling bond defects probably located at the interface between the Si substrate and the SiGe layer. A strong defect density reduction is found in correlation with the presence of Ge in the SiGe layer. A more detailed analysis suggests that this defect density reduction is caused by the out-diffusion of Ge atoms from the SiGe layer upon thermal processing.

In Chapter 5 we analyzed defects at the interfaces between Ge and different oxide insulators. However, achieving this goal does not come free of obstacles, as the commonly used capacitance and admittance based characterization techniques are inadequate to probe traps in high mobility semiconductor / oxide insulator stacks. In the first part of chapter 5 we tackled this topic by using an alternative solution, i.e., the SPV technique. Then, by measuring the D_{IT} energy distribution in a series of Ge/HfO_2 stacks passivated by Sc-doped Ge oxides, by means of both the SPV and the conventional CV and GV methods, we have confirmed previous inference that the majority of the charge trapping centers in Ge/high-k stacks are *slow* oxide traps.

We have then performed a study on a large set of Ge-based MOS capacitors of different compositions and subjected to various passivation schemes, revealing a similar D_{IT} energy distributions. Considering that interfaces of Si with the same insulators exhibit a much lower defect density, we suggest the existence of a common contribution to the D_{IT} correlated with the presence of Ge in the oxide.

Therefore, in Chapter 6 we directly addressed the defectivity of Ge-contaminated HfO_2 films by EPDS spectroscopy. The differences between the spectral charge density distributions as probed in the pristine and Ge-contaminated HfO_2 layers indicated that the presence of Ge atoms diffusing within the HfO_2 insulator introduce additional electron traps with an energy distribution which overlaps the band gap of Ge.

In conclusion, the major findings of this thesis can be concisely summarized in the following few headlines:

- The composition of a SiGe layer (namely, its Ge content) appears to play a major role in determining whether Si **or** Ge dangling bond defects are

generated at its interfaces. For the semiconductor surface orientations and strain configurations explored in our work, **no dangling bond defects** of either type (Si P_{b0} or Ge P_{b1} centers) have been found at interfaces of $Si_{1-x}Ge_x$ layers with a Ge concentration x between 28 % and 45 %.

- Strain plays a significant role in determining the electrical quality in SiGe-based devices: Whereas Ge DBs are present, strain correlates with an increased interface defect density and a reduced defect passivation efficiency by hydrogen anneal.
- The major source of traps in Ge/oxide stacks stems from defects within the oxide insulator. These traps have a much larger time constant than interface traps and may escape detection by room temperature capacitance- and conductance-based methods. Characterization by means of SPV spectroscopy leads to more reliable D_{IT} evaluation.
- A considerable contribution to the D_{IT} distribution in Ge/HfO_2 stacks stems from the presence of Ge contaminants inside the oxide layer, as well as from intrinsic oxide trapping sites.

These conclusions entail a number of consequences for the evolution of nanoelectronic devices, both from the view point of process optimization and of the understanding of reliability degradation.

Regarding the reliability, the transition from a system with charge trapping dominated by interfacial (Si(Ge)/SiO_2) defects to charge trapping by centers residing in the oxide stack, might dramatically affect the way of handling the electrical quality of the interface and assessing the reliability. In one possible scenario, the large time constant of oxide defects might imply that one trap present in a device switching at relatively high frequencies could remain inactive for some time. However, one might envision several processes (e.g., tunneling) that could induce its charging during the device lifetime. With pronounced geometric and voltage scaling, even a single charge could induce an appreciable shift of the device I_d-V_G characteristic, which might come as a fixed V_T shift. This might have a dramatic impact on the device-to-device variability in an extended circuitry.

Reducing the oxide defectivity and impeding, if possible preventing, out-diffusion of Ge atoms from the channel layer may thus be indicated as key factors on the route to achieve functional performance and high-reliability in Ge-based MOS devices -as opposed to the interface passivation concept dominating Si MOS technology.

7.2 Additional applications of the SPV technique

A last note concerns our implementation of the SPV technique. In Appendix A, it is discussed how the experimental set up for the SPV measurements has been tested on several MOS capacitors. The results show how the SPV methodology is able to reproduce D_{IT} distributions in as-oxidized and H-passivated Si/SiO_2 interfaces. Moreover, its effectiveness is also demonstrated for MOS capacitors with multi-layer semiconductors and on III-V group semiconductor interfaces.

On one hand, it is observed that the diffusion length of carriers photo-generated in Ge and III-V alloys is large enough to allow application of SPV characterization also to 3D channel FETs. This is particularly interesting considering that high levels of strain are expected at the edges and corners of the Fin channel. As we have mentioned throughout this thesis, strain correlates with enhanced Ge out-diffusion upon thermal processing, and this increases the probability of gate insulator contamination. The SPV method offers a valuable tool to investigate interface and oxide defects in these 3D structures, and thus support process optimization, since the reference flatband condition will be reached under intense illumination irrespective of the device geometry.

On the other hand, an increasingly wide field of research is being dedicated to the study of logic devices based on 2-dimensional materials (e.g. graphene, MoS_2 and so on). Promising performances have been demonstrated experimentally by combining transition metal dichalcogenides as channel material and HfO_2 as gate oxide [2]. However, looking at the energy band diagram of those devices, it appears hard to find an appreciable band bending at the interface between the 2D material and the gate insulator. This makes the SPV methodology ineffective in these cases.

Nevertheless, in the areas where the SPV methodology can find application, this is not limited to interface trap characterization. Preliminary data reported in the appendix to this thesis demonstrate that the direct sensing of the semiconductor surface potential allows detection of Fermi level pinning. The latter, whereas not evident in capacitance and admittance measurements, emerges clearly from SPV data, also resulting in an estimate of the exact energy level at which the pinning occurs (as an example, see Fig. A.5).

One more interesting application of the SPV technique concerns the semiconductor band gap width estimation. This is still a complicated task, as the most commonly used techniques rely on the observation of optical transitions and are thus limited in a number of ways. To name a few, photo- and cathodo-luminescence measurements cannot distinguish between excitonic and band-to-band transitions, and photoconductivity measurements are not straightforward in presence of a multi-layered structure in devices.

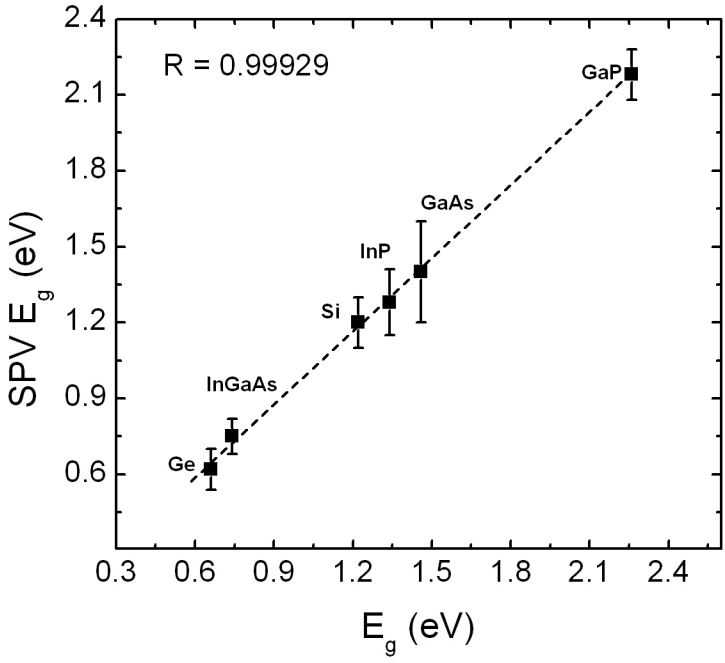


Figure 7.1: Band gap widths (solid squares) as estimated by means of SPV measurements vs. literature data (x axys). A correlation coefficient of 0.99929 is found.

Here, probing the surface potential by means of SPV measurements can offer a reliable solution. Ideally, when an MOS structure is biased in accumulation or inversion, the piling-up of charges at the semiconductor surface induces a screening effect which halts any further penetration of the applied electric field. Also, both the accumulation and inversion layers charge densities depend exponentially on the surface potential. As a result, under these conditions ψ_S hardly changes with increasing/decreasing gate bias, resulting in two plateaus in the ψ_S - V_G curve. The voltage difference between these two plateaus directly corresponds to the band gap of the semiconducting layer. Fig. 7.1 resumes preliminary data collected on a set of samples comprised of Si, Ge and several III-V semiconductor MOS capacitors with Al_2O_3 or HfO_2 insulators. There, the band gap width estimated from SPV measurements is compared with data available in the literature. A correlation factor close to 1 is found, hence suggesting that the methodology put in place is valid as long as

Fermi level pinning does not occur.

Bibliography

[1] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P.M. Ajayan, and K. Banerjee *A subthermionic tunnel field-effect transistor with an atomically thin channel* Nature, **526**, 91 (2015)

[2] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis *Single-layer MoS_2 transistors* Nature Nanotech., **6**, 147 (2011)

Appendix A

Validation and control measurements on the SPV set up

In chapter 2 we described the physical principle and experimental implementation of the Saturation surface PhotoVoltage technique. However, as mentioned before, the development of the experimental set-up required a series of test measurements in order to attest its correctness and validate the overall implementation.

In this appendix, four control experiments are discussed. First, we report on SPV measurements performed on reference (100) Si/SiO_2 capacitors and the comparison with results obtained by means of the conventional AC-conductance method. A considerable amount of literature has been published on Si/SiO_2 interface defects, which thus constituted a natural choice to be used as reference and control samples.

Second, the $\psi_S(V_G)$ relationship is probed on samples provided with multi-layered substrates. The presence of buried interfaces in the sample under investigation might be a reason of concern, as each interface will introduce a space charge region potentially contributing to the SPV signals measured at the surface (see page 47 of Ref. [1]). Here, SPV experiments were performed on a sample with a Ge *virtual substrate* on a Si carrier wafer, as well as on a Si/Ge *virtual substrate*/GeSn sample.

Third, we report on experiments performed on MOS capacitors fabricated on InGaAs epitaxially grown on a InP carrier wafer, in order to investigate the impact that the Dember (diffusion) potential might have on the SPV

experiments.

The last part illustrates a different concern about the accurate sensing of the semiconductor potential, that is, Fermi level pinning (FLP). Its signature on the SPV measurements is shown by presenting results obtained on a series of samples, fabricated on a single crystal InP substrate, provided with high-k oxide insulators of different thicknesses.

A.1 Si/SiO_2 D_{IT} determination

A.1.1 Description of samples

A first set of samples was fabricated on a (100) p-type Si wafer by dry oxidation. The final oxide thickness measured by spectroscopic ellipsometry is found to be 31 ± 1 nm. Devices were then completed by thermoresistive evaporation of semi-transparent Au electrodes of 0.5 mm^2 area on top of the oxide layer. The Si/SiO_2 interface defects were analyzed both on pristine samples and after defect passivation by annealing at 400 $^\circ C$ for 30 min in molecular hydrogen (1 atm).

A.1.2 Results

Fig. A.1(a) shows the PV transients measured for varying bias conditions on the (100) Si/SiO_2 structures after passivation treatment in molecular hydrogen. In Fig.A.1(b) the corresponding surface potential is plotted versus gate bias (open symbols), together with the surface potential curve as measured with a step size of $\Delta V_G = 0.01$ V (black curve) and the theoretical curve computed according to Ref. [2] (blue curve). The experimental $\psi_S(V_G)$ curves on the H-passivated sample is in good agreement with the theoretical one except for the deep depletion region ($V_G > 1$ V) where the low-level leakage current prevents the formation of the inversion layer, as also indicated by the CV curves presented in Fig.A.1(c). Nevertheless, SPV is still able to read the surface potential in this region. No impact is expected on the trap density estimation, since the slope of the ψ_S-V_G curve measured in depletion remains, within accuracy, unaffected by leakage (see below).

Fig. A.1(b) also shows the SPV curve measured on the Si/SiO_2 samples before the defect passivation heat treatment in molecular hydrogen (As-received, red curve). The different slope of the curves measured in the depletion gate bias range prior and after the passivation anneal reflects the contribution of unpassivated traps (Si dangling bond defects).

Finally, the D_{IT} vs E_{IT} (where E_{IT} is the interface trap energy relative to the VBT) energy distributions calculated using Eq. 2.17 are compared

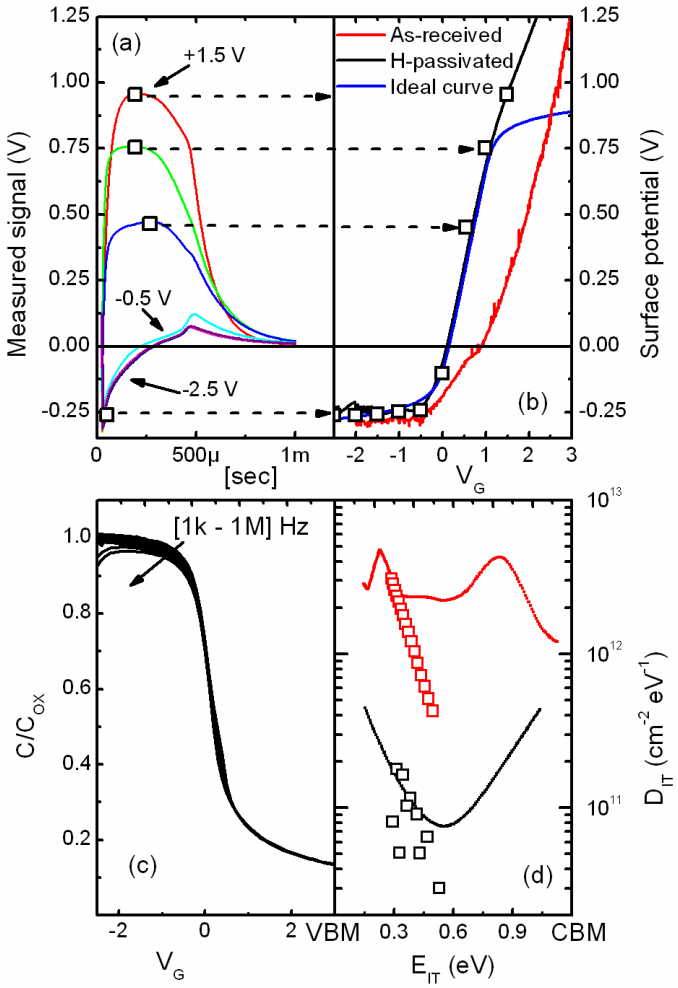


Figure A.1: (a) Plot of voltage signals vs. time measured at several gate biases (indicated numbers), on the (100)p-Si/SiO_2 after passivation annealing in H_2. The signal acquisition is set to be triggered by the falling phase of the electrical pulse generated to command the light source. Open symbols indicate the extracted surface potential values. (b) ψ_S vs. gate bias (open square symbols correspond to the signals of Fig.1(a)) as measured on the sample prior and after defects passivation in H_2 (red and black curve, respectively) and the theoretical curve as computed according to Ref. [2] by using the CVC software [4] (blue curve). (c) CV curves as measured in the frequency range 1 kHz - 1 MHz on the sample after H-passivation. (d) $D_{IT}(E_{IT})$ distributions as evaluated by SPV and AC-conductance technique (bold curves and open symbols, respectively) on the sample prior- (red curve and symbols) and after passivation anneal in H_2 (black curve and symbols).

in Fig.A.1(d) together with the ones extracted using the conventional AC-conductance method (bold curves and open symbols, respectively). The results show good overall agreement and are consistent with the (100)Si/SiO_2 defect densities reported in the literature [3]: D_{IT}s extracted from the pristine sample (red symbols in Fig.A.1(d)) are in the order of $10^{12} cm^{-2} eV^{-1}$, clearly displaying the two characteristic peaks at E_{IT} = 0.25 and 0.85 eV corresponding to the (+/0) and (0/-) transitions of the P_{b0} centers at the (100) Si/SiO_2 interface. By contrast, the densities extracted on the hydrogen-passivated sample (black symbols) are in the low $10^{11} cm^{-2} eV^{-1}$ range.

Hence, the data shown here demonstrate how SPV experiments accurately reproduce results obtained by mean of the traditional AC-conductance method. It is worth noting that, unlike the AC-conductance method, the SPV technique is able to characterize the interface defect energy distributions across the entire band gap in a sample of one silicon doping type.

A.2 Impact of buried interfaces on the SPV measurements

A.2.1 Description of samples

In this section two samples have been studied. The first sample was manufactured on a Ge VS (thickness ≥ 1 μm) epitaxially grown on a Si carrier wafer on top of a strain-relief buffer. After a HF 2% clean for 30 sec, an Al_2O_3 layer of $\approx$ 1 nm thick was deposited by ALD at 300 $^\circ C$ (10 cycles). Subsequently, O_2 plasma oxidation (800 W for 10 sec at RT) was performed through the alumina layer in order to form a Ge oxide interlayer. Finally, HfO_2 insulating cap was deposited on top by ALD at 300 C using $HfCl_4$ and water as precursors. The final thicknesses of the insulating layers were estimated by XPS to be about 1 nm for GeO_X, 0.6 nm for Al_2O_3 and 2.3 nm for HfO_2.

The second sample was prepared on a Ge VS epitaxially grown on a Si carrier wafer: on this, a lattice-matched, fully strained, GeSn layer was grown by Reduced Pressure Chemical Vapor Deposition (RPCVD) using $SnCl_4$ and Si_2H_6 as precursors. The final Sn concentration was estimated at [Sn] = 2.9 $\pm$ 0.5 % and the thickness, as estimated by RBS, was 51 nm. After HF:HCl-last surface cleaning, a 10 nm thick HfO_2 layer was deposited by ALD using tetrakismetylamino-hafium and ozone at 300 $^\circ C$. More details on the fabrication process of these samples can be found in the literature [5][6][7].

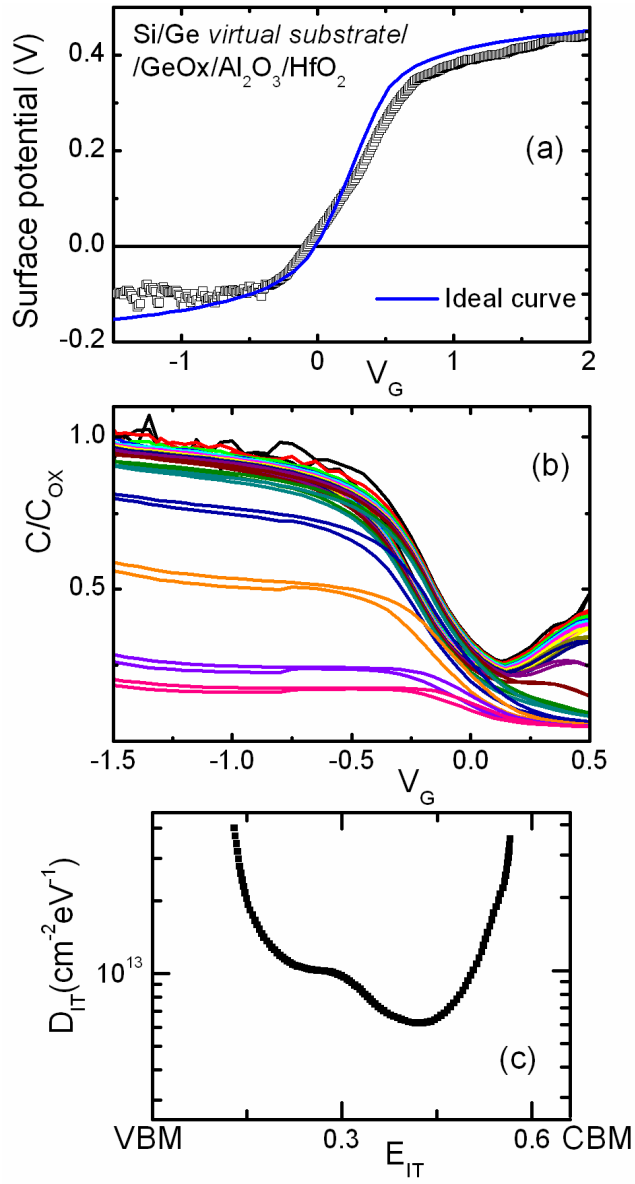


Figure A.2: (a) Surface potential versus gate bias measured by SPV on a $Si/Ge/GeO_X/Al_2O_3/HfO_2$ sample (square symbols) and as computed (blue curve) by the CVC software [4] by substituting characteristic parameters of Ge as retrieved from [8]. (b) CV curves measured in the 100 Hz to 1 MHz frequency range at room temperature. (c) D_{IT} energy distribution as estimated by means of the SPV method.

A.2.2 Results

Figure A.2(a) shows an example of SPV data as measured on a Si/Ge VS/1 nm GeO_X/0.6 nm Al_2O_3/2.3 nm HfO_2 sample (black open symbols), together with the theoretical (blue) curve computed according to Ref. [2], using the Ge bulk parameters (band gap width, intrinsic carrier concentration, and effective density of states in conduction and valence bands) and, for the oxide insulator, the measured capacitance per unit area.

The good agreement between the theoretical and experimental curves is evident and, considering that the somewhat different slope of the experimental curve is due to the effect of charge trapping, we can conclude that the presence of the buried interfaces between the Ge VS and the strain relief buffer, as well as between the buffer and the Si carrier wafer, has no measurable influence on the SPV response.

Figure A.2(b) shows the CV curves measured in the frequency range 100 Hz - 1 MHz. The presence of buried layers results in a large series resistance causing a large frequency dispersion. The lack of reliable high-frequency curves impedes *de facto* the estimation of the flat-band voltage. Also, no peaks could be resolved from the conductance response and thus no D_{IT} extraction could be performed by means of this AC conductance method. By contrast, the zero crossing of the surface potential curve measured through SPV can be found at about V_{FB} = - 0.05 ± 0.05 V which allows determination of the D_{IT} energy distribution as shown in Fig. A.2(c).

To further affirm these results, a similar analysis was performed on a Si/Ge VS/$GeSn_{0.03}$/HfO_2 sample, as illustrated in Fig. A.3(a),(b),(c). Also in this case the theoretical surface potential versus gate bias curve [blue curve in Fig. A.3(a)] was computed by using the characteristic parameters of Ge as, within the accuracy offered by the experimental set-up, the presence of 2.9 % Sn in alloy with Ge has no major effect on the semiconductor band gap width or on the surface potential span. As can be seen, the $\psi_S(V_G)$ curve measured by SPV closely agrees with the theoretical curve across the entire gate voltage span. Similar to the case study presented above, the CV / GV characteristic was found to be disturbed by a large series resistance and no D_{IT} values could be extracted; Fig. A.3(b) shows the CV curves measured in the frequency range 100 kHz to 1 MHz. As a result, Fig.A.3(c) shows only the D_{IT} density distribution as calculated from the SPV data.

In conclusion, the results discussed here indicate that the effect of buried interfaces on the measured SPV signal falls within the experimental accuracy, provided that these interfaces lie deep enough below the semiconductor/oxide

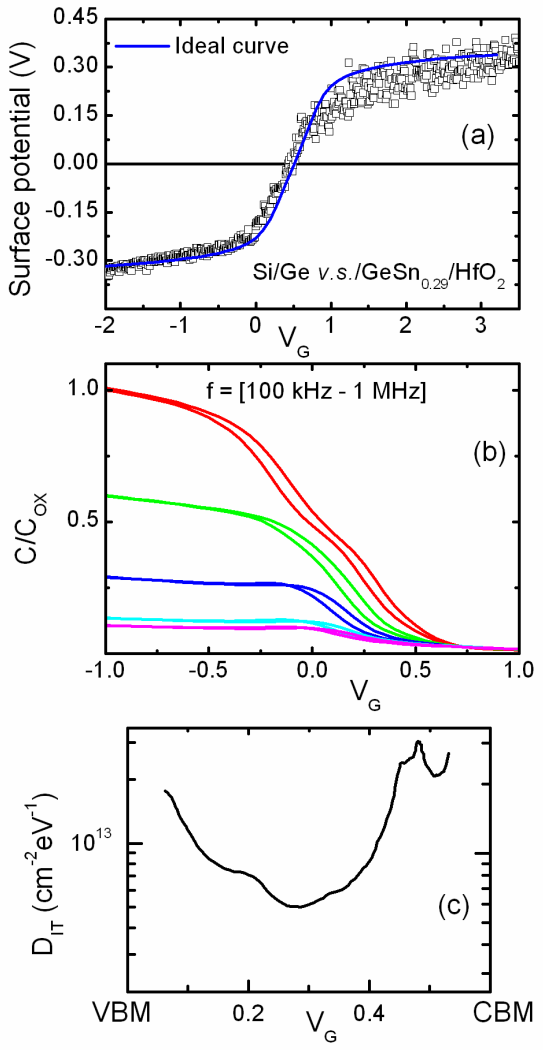


Figure A.3: (a) Surface potential versus gate bias measured by SPV on a $Si/Ge/GeSn_{0.03}/Al_2O_3/HfO_2$ sample and as computed by the CVC software [4] by substituting characteristic parameters of Ge as retrieved from [8]. (b) C-V curves measured at room temperature in the frequency range 100 kHz to 1 MHz. (c) $D_{IT}(E_{IT})$ energy distribution as extracted by means of the SPV method.

interface.

A.3 Impact of Dember potential studied on $InP/In_{0.53}Ga_{0.47}As/GdAlO_3/HfO_2$ capacitors

A.3.1 Description of samples

The sample analyzed in this section was fabricated on a (100) InP substrate with a lattice matched $In_{0.53}Ga_{0.47}As$ layer on top. The insulator processing started with ALD deposition of a 2 nm 50 % $GdAlO_3$ layer at 250 $°C$, followed by the deposition of 2 nm HfO_2 at 300 $°C$. All capacitors were completed by evaporation of semitransparent (13 nm thick) Au electrodes on top of the oxide.

A.3.2 Results

As discussed in literature [1], when excess carriers are generated in a semiconducting layer characterized by a large difference between the mobility values for electrons and holes, an additional contribution to the overall potential measured across the layer is expected. Going by the name of Dember potential, it arises in order to compensate for the charge unbalance created as a result of the different drift velocities of the two types of carriers. For this reason, it constitutes major concern for the application of the SPV characterization method to III-V semiconductor interfaces (largest differences between μ_e and μ_h, see Table 1.1). Nonetheless, as already noticed in [1], this Dember potential does not saturate with increasing carrier injection density, and hence the existence of a saturation surface PV itself is an indication that the Dember potential is negligible (the latter should increase linearly with the intensity of the incident).

To confirm the validity of this consideration, we performed SPV experiments on an $In_{0.53}Ga_{0.47}As/GdAlO_3/HfO_2$ structure fabricated on an InP substrate wafer.

Fig. A.4 shows the $\psi_S(V_G)$ curves (panel a) measured by means of the SPV technique and as computed according to Ref. [2] (black open symbols and blue solid curve, respectively), and (panel b) the CV curves measured in the frequency range 100 Hz - 1 MHz. As can be seen in Fig. A.4(a) the surface potential can be efficiently swept from accumulation to inversion and the experimental values are in good agreement with the theoretical curve.

Fig. A.4(c) shows the D_{IT} distributions as extracted by means of SPV and the conventional conductance method (black curve and open symbols, respectively). Remarkably, the two results closely agree with a mid-gap density of about D_{IT}(mid-gap) = (5 $\pm$ 1) x $10^{12}(cm^{-2}eV^{-1})$.

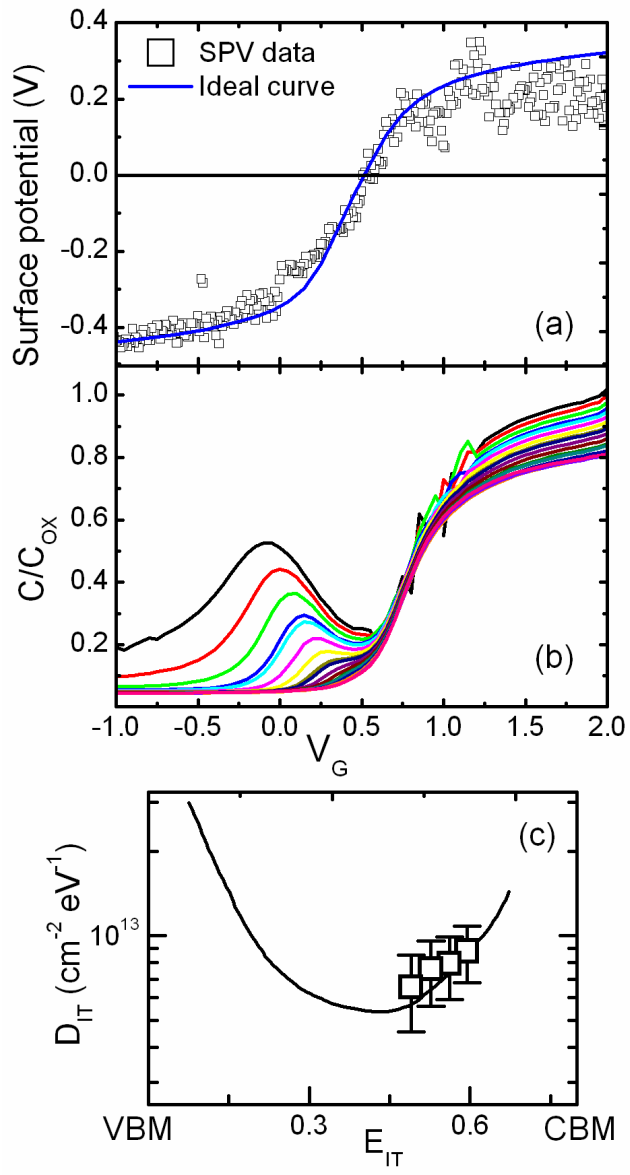


Figure A.4: (a) Surface potential vs gate bias $\psi_S(V_G)$ curves as measured through the SPV technique (open symbols) and as computed by the CVC software [4] (blue curve) by using the semiconductor parameters as retrieved from Ref. [8]. (b) Resume of the CV curves as measured in the frequency range 100 Hz - 1MHz on the InP/$In_{0.53}Ga_{0.47}As$/2 nm $GdAlO_3$/2 nm HfO_2 sample. (c) The D_{IT} distributions estimated by the SPV technique (black curve) and by mean of the AC conductance method (open squares).

All considered, we found no evidence for the presence of significant additional contribution provided by the Dember potential to the measured SPV.

A.4 Impact of strong Fermi level pinning

A.4.1 Description of samples

Samples were fabricated on a (100) InP substrate. On the first sample S01 2 nm Al_2O_3 + 2 nm HfO_2 have been deposited. On other two samples S02 and S03, the insulating stack comprised of 2nm $GdAlO_3$ and 2nm HfO_2 on sample S02 and 4 nm $GdAlO_3$ and 2 nm HfO_2 on sample S03, respectively. The last sample S04 was provided with only 10 nm $GdAlO_3$. All capacitors were completed by evaporation of semitransparent (13 nm thick) Au electrodes on top of the oxide.

A.4.2 Results

The inefficient E_F sweep across the semiconductor band gap caused by the presence of interface states that is, the Fermi Level Pinning (FLP), is among major concerns for III-V based MOSFET devices realization. Nonetheless, recognition of FLP on the sole base of capacitance or admittance measurements is an arduous task.

Fig. A.5(a) shows the CV curves as measured on sample S03, fabricated on InP with 4 nm $GdAlO_3$ and 2 nm HfO_2 as oxide insulator, in the frequency range between 100 Hz and 1MHz. Samples 01, 02 and 04, part of this same set exhibit similar features on the CV curves (not shown). The frequency-dependent dispersion in the accumulation condition and the frequency-dependent shift of the flat-band voltage affecting the CV curves (indicated by an arrow in Fig. A.5(a)) have been associated with weak FLP [9].

Fig. A.5(b) shows the $\psi_S(V_G)$ curves as measured using the SPV method on samples S01 to S04, together with the theoretical curve as computed by [4]. As can be seen from the CV characteristic in Fig. A.5(a) and confirmed by the computed ideal curve in Fig. A.5(b), the MOS structures are expected to reach inversion for gate biases below -1V. By contrast, the experimental SPV curves in Fig. A.5(b) appear to reach a plateau as the gate bias becomes negative (at the gate potential between -0.4V and -0.6V). Beyond this voltage range the curves are seen to drop reaching another plateau at a potential of about -1.2V. Further increase of the gate bias is seen to cause the dielectric breakdown.

Importantly, the voltage at which ψ_S drops correlates with the thickness of the insulating oxide: A higher negative voltage is needed to induce the leakage and cause inequilibrium depletion in samples provided with a thicker insulator.

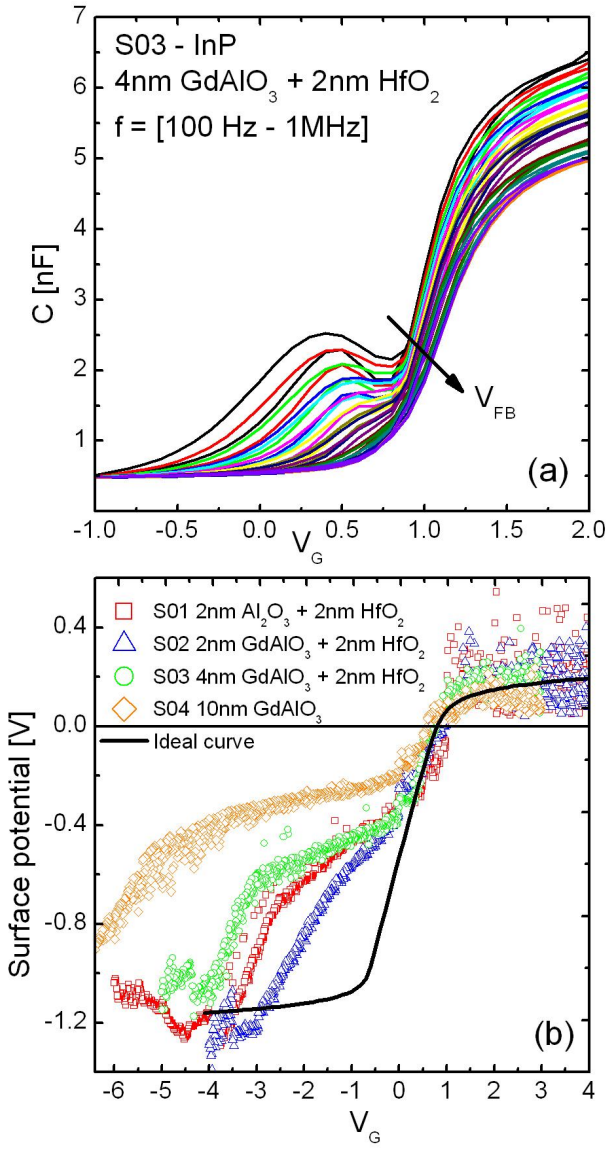


Figure A.5: (a) Capacitance versus gate voltage curves as measured, in the frequency range 100Hz – 1MHz, on sample S04, representing the key features of the CV curves as measured on all samples of this sub-set. No FLP can be unquestionably identified on the pure basis of this CV characteristic. (b) ψ_S versus V_G curves as measured by mean of SPV experiments on samples S01 to S04, together with the ideal curve as computed by the CVC software [4]. The Fermi level appears to be pinned at a position between 0.6 eV and 0.8 eV below the InP conduction band.

The dependence of these curves with respect the oxide thickness indicates that the first plateau on the $\psi_S(V_G)$ curves is caused by a FLP at about 0.6eV to 0.8 eV below the InP conduction band.

Samples with thicker oxides are able to endure higher electric fields (as a reference, for 4 nm oxide insulator, a gate bias of -3V results in 7.5 MV/cm of electric field strenght).

Likewise, the different curves evaluated on samples S01 and S02, provided with the same overall thickness of the insulating layer but with different composition, can be explained by reduced leakage current affecting the sample provided with a Gd-free insulator.

This result confirms previous research performed on the same samples [10] whose results revealed the formation of an In-rich inter-layer in between the (100)InP substrate and the oxide insulator. The conceivable high-defectivity of such inter-layer might be the cause of the revealed FLP.

Bibliography

[1] L. Kronik, and Y. Shapira *Surface Photovoltage Phenomena: theory, experiment, and applications* Surf. Sci. Rep., **37**, 1 (1999)

[2] E.H. Nicollian, and J.R. Brews *MOS(Metal Oxide Semiconductor) Physics and Technology* (Wiley-Interscience, NewYork, 1982)

[3] N.H. Thoan, K. Keunen, V.V. Afanas'ev, and A. Stesmans *Interface state energy distribution and P_b defects at (110)Si/SiO_2 interfaces: Comparison to (111) and (100) silicon orientations* J. Appl. Phys., **109**, 013710 (2011)

[4] J.R. Hauser, CVC software, http://ece.ncsu.edu/research/tool

[5] S. Wirths, R. Geiger, N.V. Den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chiussi, J.M. Hartmann, H. Sigg, J. Faist, D. Buca, and D. Grützmacher, Nature Photonics, **9**(2), 88 (2015)

[6] S. Wirths, D. Stange, M.A. Pampillon, A.T. Tiedemann, G. Mussler, A. Fox, U. Breuer, B. Baert, E. San Andres, N.D. Nguyen, J.M. Hartmann, Z. Ikonic, S. Mantl, and D. Buca, ACS Appl. Mater. Interfaces, **7**, 62 (2015)

[7] N. Von Den Driesch, D. Stange, S. Wirths, G. Mussler, B. Hollander, Z. Ikonic, J. M. Hartmann, T. Stoica, S. Mantl, D. Grutzmacher, and D. Buca, *Direct Bandgap Group IV Epitaxy on Si for Laser Applications* Chem. Mater., **27**, 4693 (2015)

[8] Electronic database, Ioffe Institute, St.Petersburg, http://www.ioffe.rssi.ru/SVA/NSM/Semicond/

[9] K. Martens, W. Wang, K. De Keersmaecker, G. Borghs, G. Groeseneken, and H. Maes, *Impact of weak Fermi-level pinning on the correct interpretation of III-V MOS C-V and G-V characteristics* Microelectron. Eng. **84**, 2146 (2007)

[10] H.Y. Chou, V.V. Afanas'ev, A. Stesmans, H.C. Lin, P.K. Hurley, and S.B. Newcomb, *Electron band alignment between (100)InP and atomic-layer deposited Al_2O_3* Appl. Phys. Lett. **97**, 132112 (2010)

List of publications

- **O. Madia**, V.V. Afanas'ev, D. Cott, H. Arimura, C. Schulte-Braucks, H.C. Lin, D. Buca, N. Von Den Driesch, L. Nyns, T. Ivanov, D. Cuypers, and A. Stesmans *Saturation Photo-Voltage methodology for semiconductor/insulator interface trap spectroscopy* ECS J. Solid State Sci. Tech., **5**(4), 3031 (2016)

- **O. Madia**, V.V. Afanas'ev, J.A. Kittl, W.K. Hong, S.S. Kim, H.Y. Lee, S. Kim, M.S. Rodder, and A. Stesmans *Germanium-related deep electron traps in ALD-grown HfO_2 insulators studied through Exhaustive PhotoDepopulation Spectroscopy* Microelectr. Eng., **147**, 188 (2015)

- **O. Madia**, N. Segercrantz, V. Afanas'ev, A. Stesmans, L. Souriau, J. Slotte, and F. Tuomisto *Charge transition level of GeP_{b1} centers at interfaces of $SiO_2/Ge_xSi_{1-x}/SiO_2$ heterostructures investigated by positron annihilation spectroscopy* Phys. Stat. Solidi B, **251**(11), 2211 (2014)

- **O. Madia**, A.P.D.Nguyen, N.H.Thoan, V.V. Afanas'ev, A. Stesmans, L. Souriau, J. Slotte, and F. Tuomisto *Impact of strain on passivation efficiency of Ge dangling bond defects in $SiO_2/Si_{1-X}Ge_X/SiO_2$ heterostructures* Appl. Surf. Sci., **291**, 11 (2014)

- **O. Madia**, J. Kepa, V.V. Afanas'ev, J. Franco, B. Kaczer, A. Hikavyy, and A. Stesmans *Si P_{b0} interface defects in Si/SiGe/HfO_2 heterostructures with nm-thin Si passivation: Defect density reduction caused by Ge out-diffusion* J. Vac. Sci. Technol (to be submitted)

- S. Gupta, E. Simoen, R. Loo, **O. Madia**, H.C. Lin, C. Merckling, Y. Shimura, T. Conard, J. Lauwaert, H. Vrielinck, and M. Heyns *Density and capture cross-sections of interface traps in $GeSnO_2$ and GeO_2 grown on hetero-epitaxial GeSn* ACS Appl. Mater. Interfaces, **8**(21), 13181 (2016)

- F. Cerbu, **O. Madia**, D. Andreev, S. Fadida, M. Eizenberg, L. Breuil, J. Lisoni, J. Kittl, J. Strand, A. Shluger, V.V. Afanas'ev, M. Houssa,

and A. Stesmans *Intrinsic electron traps in atomic-layer deposited HfO_2 insulators* Appl. Phys. Lett. **108**, 222901 (2016)

- N.M. Kolomiiets, V.V. Afanas'ev, **O. Madia**, H. Arimura, D. Cott, N. Collaert, A. Thean, and A. Stesmans *Effect of La doping on interface barrier between Si-passivated Ge and insulating HfO_2* Phys. Stat. Solidi C, (Submitted to Physica Status Solidi C)

- V.V. Afanas'ev, W.C. Wang, F. Cerbu, **O. Madia**, M. Houssa, and A. Stesmans *(Invited) Spectroscopy of Deep Gap States in High-k Insulators* ECS Trans., **64**(8), 17 (2014)

- B. Kaczer, V.V. Afanas'ev, K. Rott, F. Cerbu, J. Franco, W. Goes, T. Grasser, **O. Madia**, A.P.D. Nguyen, A. Stesmans, H. Reisinger, M. Toledano-Luque, and P. Weckx *Experimental characterization of BTI defects* International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 444 (2013)

Conference contributions

- **O. Madia**, A.P.D. Nguyen, N.H. Thoan, V.V. Afanas'ev A. Stesmans, L. Souriau, J. Slotte, F. Tuomisto *Impact of strain on the passivation efficiency of Ge dangling bond interface defects in condensation grown $SiO_2/Si_{1-x}Ge_x/SiO_2/(100)Si$ structures with nm-thin $Si_{1-x}Ge_x$ layers*

  E-MRS Spring meeting 2013, Strasbourg (France), May 2013

- **O. Madia**, A.P.D. Nguyen, N.H. Thoan, V.V. Afanas'ev A. Stesmans, L. Souriau, J. Slotte, F. Tuomisto *Impact of strain on the passivation efficiency of Ge dangling bond interface defects in condensation grown $SiO_2/Si_{1-x}Ge_x/SiO_2/(100)Si$ structures with nm-thin $Si_{1-x}Ge_x$ layers*

  COST CM1104 WG4 meeting, London (UK), May 2013

- **O. Madia**, A.P.D. Nguyen, N.H. Thoan, V.V. Afanas'ev A. Stesmans, L. Souriau, J. Slotte, F. Tuomisto *Impact of strain on the passivation efficiency of Ge dangling bond interface defects in condensation grown $SiO_2/Si_{1-x}Ge_x/SiO_2/(100)Si$ structures with nm-thin $Si_{1-x}Ge_x$ layers*

  COST CM1104 General Meeting, Uppsala (Sweden), Nov. 2013

- **O. Madia**, J. Kepa, F. Cerbu, V.V. Afanas'ev, M. Houssa, A. Stesmans *Si P_{b0} defects at interfaces of Si-passivated SiGe channels with HfO_2*

  COST CM1104 WG4 Meeting, Riga (Latvia), Apr. 2014

- **O. Madia**, N. Segercrantz, V.V. Afanas'ev, A. Stesmans, L. Souriau, J. Slotte, F. Tuomisto *Charge transition level of Ge P_{b1} centers at interfaces of $SiO_2/Si_{1-x}Ge_x/SiO_2$ heterostructures investigated by positron annihilation spectroscopy*

  E-MRS Spring meeting 2014, Lille (France), May 2014

- **O. Madia**, J. Kepa, V.V. Afanas'ev, M. Houssa, A. Stesmans *Si dangling bonds at interfaces of Si-passivated SiGe channels with HfO_2*

  MORDRED M36 meeting, London (UK), Sep. 2014

- O. Madia, J. Kepa, F. Cerbu, V.V. Afanas'ev, M. Houssa, A. Stesmans *Oxygen scavenging-induced Si P_{b0} defects at interfaces of Si-passivated SiGe channels with HfO_2*

  COST CM1104 General Meeting, Barcelona (Spain), Nov. 2014

- **O. Madia**, V.V. Afanas'ev, J.A. Kittl, W.K. Hong, S.-S. Kim, H.Y. Lee, S. Kim, M.S. Rodder, A. Stesmans *Germanium-related deep electron traps in ALD-grown HfO_2 insulators studied by Exhaustive PhotoDepopulation Spectroscopy*

  INFOS 2015, Udine (Italy), Jun. 2015

- N.M. Kolomiiets, V.V. Afanas'ev, **O. Madia**, H. Arimura, D. Cott , N. Collaert , A. Thean , A. Stesmans *Effect of La doping on interface barrier between Si-passivated Ge and insulating HfO_2*

  E-MRS Spring Meeting 2016, Lille (France), May 2016

FACULTY OF SCIENCE
DEPARTMENT OF PHYSICS AND ASTRONOMY
SEMICONDUCTOR PHYSICS RESEARCH LABORATORY
Celestijnenlaan 200D
B-3001 Leuven
oreste.madia@fys.kuleuven.be
www.website.kuleuven.be